Mathematics-III for EE Engineering			
Course Code	**BMATE 301**	CIE Marks	50
Teaching Hours/Week (L:T:P: S)	3:1:0:0	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	03	Exam Hours	03
Examination type (SEE)	Theory		

Course objectives:

- To acquaint the students with differential equations and their applications in electrical engineering
- To find the association between attributes and the correlation between two variables
- Learn to use Fourier series to represent periodical physical phenomena in engineering analysis and to enable the student to express non periodic functions to periodic function using Fourier series and Fourier transforms.
- To learn the basic ideas of the theory of probability and random signals.

Teaching-Learning Process (General Instructions)

These are sample Strategies; which teachers can use to accelerate the attainment of the various course outcomes.

1. Lecturer method (L) needs not to be only traditional lecture method, but alternative effective teaching methods could be adopted to attain the outcomes.
2. Use of Video/Animation to explain functioning of various concepts.
3. Encourage collaborative (Group Learning) Learning in the class.
4. Ask at least three HOT (Higher order Thinking) questions in the class, which promotes critical thinking.
5. Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop design thinking skills such as the ability to design, evaluate, generalize, and analyse information rather than simply recall it.
6. Introduce Topics in manifold representations.
7. Show the different ways to solve the same problem with different circuits/logic and encourage the students to come up with their own creative ways to solve them.
8. Discuss how every concept can be applied to the real world - and when that's possible, it helps improve the students' understanding.

Module-1 :Ordinary Differential Equations of Higher Order (8 hours)

Importance of higher-order ordinary differential equations in Electrical & Electronics Engineering applications.

Higher-order linear ODEs with constant coefficients - Inverse differential operator, problems.Linear differential equations with variable Coefficients-Cauchy's and Legendre's differential equations - Problems.

Applications: Application of linear differential equations to L-C circuit and L-C-R circuit.

Self-Study: Finding the solution by the method of undetermined coefficients and method of variation of parameters.

(RBT Levels: L1, L2 and L3)

Module-2: Curve fitting, Correlation and regressions

Principles of least squares, Curve fitting by the method of least squares in the form $y = a + bx$, $y = a + bx + cx^2$, and $y = ax^b$. Correlation, Co-efficient of correlation, Lines of regression, Angle between regression lines, standard error of estimate, rank correlation

Self-study: Fitting of curves in the form $y = a\, e^{bx}$

Module-3 Fourier series.
Periodic functions, Dirchlet's condition, conditions for a Fourier series expansion, Fourier series of functions with period 2π and with arbitrary period. Half rang Fourier series. Practical harmonic analysis. **Application to variation of periodic current.** **Self-study:** Typical waveforms, complex form of Fourier series
Module-4 Fourier transforms and Z -transforms
Infinite Fourier transforms: Definition, Fourier sine, and cosine transform. Inverse Fourier transforms Inverse Fourier cosine and sine transforms. Problems. **Z-transforms:** Definition, Standard z-transforms, Damping, and shifting rules, Problems. Inverse z-transform and applications to solve difference equations **Self-study**: Convolution theorems of Fourier and z-transforms
Module-5 Probability distributions
Review of basic probability theory, Random variables-discrete and continuous Probability distribution function, cumulative distribution function, Mathematical Expectation, mean and variance, Binomial, Poisson,Exponential and Normal distribution (without proofs for mean and SD) – Problems. **Sampling Theory:** Introduction to sampling distributions, standard error, Type-I and Type-II errors.Student's t-distribution, Chi-square distribution as a test of goodness of fit. **Self-study:** Test of hypothesis for means, single proportions only.
Course outcome (Course Skill Set)
At the end of the course, the student will be able to : 1. Understand that physical systems can be described by differential equations and solve such equations 2. Make use of correlation and regression analysis to fit a suitable mathematical model for statistical data 3. Demonstrate the Fourier series to study the behavior of periodic functions and their applications in system communications, digital signal processing, and field theory. 4. To use Fourier transforms to analyze problems involving continuous-time signals and to apply Z-Transform techniques to solve difference equations 5. Apply discrete and continuous probability distributions in analyzing the probability models arising in the engineering field. Demonstrate the validity of testing the hypothesis.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). The student is declared as a pass in the course if he/she secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

- There are 25 marks for the CIE's Assignment component and 25 for the Internal Assessment Test component.
- Each test shall be conducted for 25 marks. The first test will be administered after 40-50% of the coverage of the syllabus, and the second test will be administered after 85-90% of the coverage of the syllabus. The average of the two tests shall be scaled down to 25 marks
- Any two assignment methods mentioned in the 22OB2.4, if an assignment is project-based then only one assignment for the course shall be planned. The schedule for assignments shall be planned properly by the course teacher. The teacher should not conduct two assignments at the end of the semester if two assignments are planned. Each assignment shall be conducted for 25 marks. (If two assignments are conducted then the sum of the two assignments shall be scaled down to 25 marks)
- The final CIE marks of the course out of 50 will be the sum of the scale-down marks of tests and assignment/s marks.

Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester-End Examination:

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (**duration 03 hours).**

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
3. The students have to answer 5 full questions, selecting one full question from each module.
4. Marks scored shall be proportionally reduced to 50 marks

Suggested Learning Resources:

Books (Title of the Book/Name of the author/Name of the publisher/Edition and Year)

Text Books

1. **B. S. Grewal**: "Higher Engineering Mathematics", Khanna Publishers, 44thEd., 2021.
2. **E. Kreyszig**: "Advanced Engineering Mathematics", John Wiley & Sons, 10thEd., 2018.

Reference Books

1. **V. Ramana:** "Higher Engineering Mathematics" McGraw-Hill Education, 11th Ed., 2017
2. **Srimanta Pal & Subodh C.Bhunia**: "Engineering Mathematics" Oxford University Press, 3rdEd., 2016.
3. **N.P Bali and Manish Goyal**: "A Textbook of Engineering Mathematics" Laxmi Publications, 10thEd., 2022.
4. **C. Ray Wylie, Louis C. Barrett:** "Advanced Engineering Mathematics" McGraw – Hill Book Co., New York, 6th Ed., 2017.

5. **Gupta C.B, Sing S.R and Mukesh Kumar:** "Engineering Mathematic for Semester I and II", Mc-Graw Hill Education(India) Pvt. Ltd 2015.
6. **H.K. Dass and Er. Rajnish Verma:** "Higher Engineering Mathematics" S.Chand Publication, 3rd Ed.,2014.
7. **James Stewart: "**Calculus" Cengage Publications, 7thEd., 2019.

Web links and Video Lectures (e-Resources):

http://nptel.ac.in/courses.php?disciplineID=111
- http://www.class-central.com/subject/math(MOOCs)
- http://academicearth.org/
- VTU e-Shikshana Program

VTU EDUSAT Program.

Activity Based Learning (Suggested Activities in Class)/ Practical Based Learning

Activity-Based Learning (Suggested Activities in Class)/Practical-Based Learning

- Quizzes
- Assignments
- Seminar

Electric Circuit Analysis			
IPCC Course Code	**BEE302**	CIE Marks	50
Teaching Hours/Week (L:T:P: S)	3:0:2:0	SEE Marks	50
Total Hours of Pedagogy	40 hours Theory +10 hrs (Lab)	Total Marks	100
Credits	4 Credits	Exam Hours	3 hrs

Course objectives:

- To familiarize the basic laws, source transformations, theorems and the methods of analyzing electrical circuits.
- To explain the use of network theorems and the concept of resonance.
- To familiarize the analysis of three-phase circuits, two port networks and networks with non-sinusoidal inputs.
- To explain the importance of initial conditions, their evaluation and transient analysis of R-L and R-C circuits.
- To impart basic knowledge on network analysis using Laplace transforms.

Teaching-Learning Process (General Instructions)

These are sample Strategies; which teachers can use to accelerate the attainment of the various course outcomes.

1. Lecturer method (L) needs not to be only traditional lecture method, but alternative effective teaching methods could be adopted to attain the outcomes.
2. Use of Video/Animation to explain functioning of various concepts.
3. Encourage collaborative (Group Learning) Learning in the class.
4. Ask at least three HOT (Higher order Thinking) questions in the class, which promotes critical thinking.
5. Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop design thinking skills such as the ability to design, evaluate, generalize, and analyse information rather than simply recall it.
6. Introduce Topics in manifold representations.
7. Show the different ways to solve the same problem with different circuits/logic and encourage the students to come up with their own creative ways to solve them.
8. Discuss how every concept can be applied to the real world - and when that's possible, it helps improve the students' understanding.

MODULE-1

Basic Concepts: Active and passive elements, Concept of ideal and practical sources. star – delta transformation.

Analysis of networks by (i) Network reduction method including, (ii) Mesh and Node voltage methods for ac and DC circuits with independent and dependent sources. Concept of Super-Mesh and Super node analysis, Duality.

Teaching-Learning Process	Chalk and Board, Problem based learning.

MODULE-2

Network Theorems: Super Position theorem, Thevenin's theorem, Norton's theorem, and Maximum power transfer theorem. (Problems with independent AC and DC sources only).

Teaching-Learning Process	Chalk and Board, Problem based learning.

MODULE-3

Resonant Circuits: Analysis of simple series RLC and parallel RLC circuits under resonances.

Problems on Resonant frequency, Bandwidth and Quality factor at resonance

Transient Analysis: Behavior of circuit elements under switching action, Evaluation of initial conditions.

Transient analysis of RL and RC circuits under DC excitations.

Teaching-Learning Process	Chalk and Board, Problem based learning.

MODULE-4

Laplace Transformation: Laplace transformation (LT), Initial and Final value theorems. Solution of electrical circuits using LT.

Teaching-Learning Process	Chalk and Board, Problem based learning.

MODULE 5

Unbalanced Three Phase Systems: Analysis of three phase systems (3-wire and 4 wire systems), calculation of real and reactive Powers.
Two Port networks: Definition, Open circuit impedance, Short circuit admittance and Transmission parameters and their evaluation for simple circuits.

Teaching-Learning Process	Chalk and Board, Problem based learning.

Practice (Laboratory) Part

Sl. No	**Experiments (to be carried out using discrete components)**
1	Study of the effect of Open and Short circuits in simple circuits.
2	Determination of resonant frequency, bandwidth, and Q of a series circuit.
3	Determination of resonant frequency, bandwidth, and Q of a parallel circuit.
4	Verification of Thevenin's theorem.
5	Verification of Norton's theorem.
6	Verification of Superposition theorem.
7	Verification of maximum Power transfer theorem.
8	Power factor correction.
9	Measurement of time constant of an RC circuit.
10	Measurement of power in three phase Circuits using two watt meter method.

Course outcomes (Course Skill Set):
At the end of the course the student will be able to:

1. Understand the basic concepts, basic laws and methods of analysis of DC and AC networks and reduce the complexity of network using source shifting, source transformation and network reduction using transformations.
2. Solve complex electric circuits using network theorems.
3. Discuss resonance in series and parallel circuits and also the importance of initial conditions and their evaluation.
4. Synthesize typical waveforms using Laplace transformation.
5. Solve unbalanced three phase systems and also evaluate the performance of two port networks.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

CIE for the theory component of IPCC

- IPCC means practical portion integrated with the theory of the course.
- CIE marks for the theory component are **25 marks** and that for the practical component is **25 marks**.
- 25 marks for the theory component are split into **15 marks** for two Internal Assessment Tests (Two Tests, each of 15 Marks with 01-hour duration, are to be conducted) and **10 marks** for other assessment methods mentioned in 22OB4.2. The first test at the end of 40-50% coverage of the syllabus and the second test after covering 85-90% of the syllabus.
- Scaled-down marks of the sum of two tests and other assessment methods will be CIE marks for the theory component of IPCC (that is for **25 marks)**.
- The student has to secure 40% of 25 marks to qualify in the CIE of the theory component of IPCC.

CIE for the practical component of IPCC

- **15 marks** for the conduction of the experiment and preparation of laboratory record, and **10 marks** for the test to be conducted after the completion of all the laboratory sessions.

- On completion of every experiment/program in the laboratory, the students shall be evaluated including viva-voce and marks shall be awarded on the same day.
- The CIE marks awarded in the case of the Practical component shall be based on the continuous evaluation of the laboratory report. Each experiment report can be evaluated for 10 marks. Marks of all experiments' write-ups are added and scaled down to **15 marks**.
- The laboratory test **(duration 02/03 hours)** after completion of all the experiments shall be conducted for 50 marks and scaled down to **10 marks.**
- Scaled-down marks of write-up evaluations and tests added will be CIE marks for the laboratory component of IPCC for **25 marks**.
- The student has to secure 40% of 25 marks to qualify in the CIE of the practical component of the IPCC.

SEE for IPCC

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (**duration 03 hours**)

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
3. The students have to answer 5 full questions, selecting one full question from each module.
4. Marks scored by the student shall be proportionally scaled down to 50 Marks

The theory portion of the IPCC shall be for both CIE and SEE, whereas the practical portion will have a CIE component only. Questions mentioned in the SEE paper may include questions from the practical component.

Suggested Learning Resources:

1. Engineering Circuit Analysis, William H Hayt et al, Mc Graw Hill,8th Edition,2014.
2. Network Analysis, M.E. Vanvalkenburg, Pearson, 3rd Edition,2014.
3. Fundamentals of Electric Circuits, Charles K Alexander Matthew N O Sadiku, Mc Graw Hill, 5th Edition, 2013.

Activity Based Learning (Suggested Activities in Class)/ Practical Based learning

Activity Based Learning, Quizzes, Seminars.

Analog Electronic Circuits			
Course Code	BEE303	CIE Marks	50
Teaching Hours/Week (L:T:P: S)	3:0:2:0	SEE Marks	50
Total Hours of Pedagogy	40 hours Theory + 8-10 Lab slots	Total Marks	100
Credits	04	Exam Hours	03
Examination nature (SEE)	Theory		

Course objectives:

- To provide the knowledge for the analysis of transistor biasing and thermal stability circuits.
- To develop skills to design the electronic circuits like amplifiers, power amplifiers and oscillators.
- To understand the importance of FET and MOSFET and FET/MOSFET amplifiers

Teaching-Learning Process (General Instructions)

These are sample Strategies; that teachers can use to accelerate the attainment of the various course outcomes.

1. Lecturer method (L) needs not to be only traditional lecture method, but alternative effective teaching methods could be adopted to attain the outcomes.
2. Use of Video/Animation to explain functioning of various concepts.
3. Encourage collaborative (Group Learning) Learning in the class.
4. Ask at least three HOT (Higher order Thinking) questions in the class, which promotes critical thinking.
5. Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop design thinking skills such as the ability to design, evaluate, generalize, and analyze information rather than simply recall it.
6. Introduce Topics in manifold representations.
7. Show the different ways to solve the same problem with different circuits/logic and encourage the students to come up with their own creative ways to solve them.
8. Discuss how every concept can be applied to the real world-and when that's possible, it helps improve the students' understanding.

MODULE-1

Diode Circuits: Diode clipping and clamping circuits.

Transistor Biasing and Stabilization:

The operating point, load line analysis, DC analysis and design of fixed bias circuit, emitter stabilized bias circuit, collector to base bias circuit, voltage divider bias circuit, modified DC bias with voltage feedback.

Bias stabilization and stability factors for fixed bias circuit, collector to base bias circuit and voltage divider bias circuit, bias compensation, Transistor switching circuits.

MODULE-2

Transistor at Low Frequencies:

Hybrid model, h-parameters for CE, CC and CB modes, mid-band analysis of single stage amplifier, simplified hybrid model, analysis for CE, CB and CC(emitter voltage follower circuit) modes, Millers Theorem and its dual, analysis for collector to base bias circuit and CE with un bypassed emitter resistance.

Transistor frequency response:

General frequency considerations, effect of various capacitors on frequency response, Miller effect capacitance, high frequency response, hybrid - pi model, CE short circuit current gain using hybrid pi model, multistage frequency effects.

MODULE-3

Multistage amplifiers:

Cascade connection , analysis for CE-CC mode, CE-CE mode, CASCODE stage-unbypassed and bypassed emitter resistance modes, Darlington connection using h-parameter model.

Feedback Amplifiers:

Classification of feedback amplifiers, concept of feedback, general characteristics of negative feedback amplifiers, Input and output resistance with feedback of various feedback amplifiers, analysis of different practical feedback amplifier circuits.

MODULE-4
Power Amplifiers: Classification of power amplifiers, Analysis of class A, Class B, class C and Class AB amplifiers, Distortion in power amplifiers, second harmonic distortion, harmonic distortion in Class B amplifiers, cross over distortion and elimination of cross over distortion. **Oscillators:** Concept of positive feedback, frequency of oscillation for RC phase oscillator, Wien Bridge oscillator, Tuned oscillator circuits, Hartley oscillator, Colpitt's oscillator , crystal oscillator and its types.
MODULE-5
FETs: Construction, working and characteristics of JFET and MOSFET(enhance and Depletion type) Biasing of JFET and MOSFET. Fixed bias configuration, self bias configuration, voltage divider biasing. Analysis and design of JFET (only common source configuration with fixed bias) and MOSFET amplifiers.

PRACTICAL COMPONENT OF IPCC

Sl.NO	Experiments
1	Experiments on series, shunt and double ended clippers and clampers.
2	Design, simulation and Testing of Full wave – centre tapped transformer type and Bridge type rectifier circuits with and without Capacitor filter. Determination of ripple factor, regulation and efficiency.
3	Static Transistor characteristics for CE, CB and CC modes and determination of h parameters.
4	Frequency response of single stage BJT and FET RC coupled amplifier and determination of half power points, bandwidth, input and output impedances.
5	Design and testing of BJT -RC phase shift oscillator for given frequency of oscillation.
6	Design, simulation (MATLAB) and testing of Wien bridge oscillator for given frequency of oscillation
7	Design and testing of Hartley and Colpitt's oscillator for given frequency of oscillation
8	Determination of gain, input and output impedance of BJT Darlington emitter follower with and without bootstrapping.
9	Design and testing of Class A and Class B power amplifier and to determine conversion efficiency.
10	Design and simulation of Full wave – centre tapped transformer type and Bridge type rectifier circuits with and without Capacitor filter using MATLAB. Determination of ripple factor, regulation and efficiency.

Course outcomes (Course Skill Set):

At the end of the course, the student will be able to:

1. Utilize the characteristics of transistor for different applications.
2. Design and analyze biasing circuits for transistor.
3. Design, analyze and test transistor circuitry as amplifiers and oscillators

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE

(Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

CIE for the theory component of the IPCC (maximum marks 50)

- IPCC means practical portion integrated with the theory of the course.
- CIE marks for the theory component are **25 marks** and that for the practical component is **25 marks**.
- 25 marks for the theory component are split into **15 marks** for two Internal Assessment Tests (Two Tests, each of 15 Marks with 01-hour duration, are to be conducted) and **10 marks** for other assessment methods mentioned in 22OB4.2. The first test at the end of 40-50% coverage of the syllabus and the second test after covering 85-90% of the syllabus.
- Scaled-down marks of the sum of two tests and other assessment methods will be CIE marks for the theory component of IPCC (that is for **25 marks)**.
- The student has to secure 40% of 25 marks to qualify in the CIE of the theory component of IPCC.

CIE for the practical component of the IPCC

- **15 marks** for the conduction of the experiment and preparation of laboratory record, and **10 marks** for the test to be conducted after the completion of all the laboratory sessions.
- On completion of every experiment/program in the laboratory, the students shall be evaluated including viva-voce and marks shall be awarded on the same day.
- The CIE marks awarded in the case of the Practical component shall be based on the continuous evaluation of the laboratory report. Each experiment report can be evaluated for 10 marks. Marks of all experiments' write-ups are added and scaled down to **15 marks**.
- The laboratory test **(duration 02/03 hours)** after completion of all the experiments shall be conducted for 50 marks and scaled down to **10 marks.**
- Scaled-down marks of write-up evaluations and tests added will be CIE marks for the laboratory component of IPCC for **25 marks**.
- The student has to secure 40% of 25 marks to qualify in the CIE of the practical component of the IPCC.

SEE for IPCC

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (**duration 03 hours**)

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
3. The students have to answer 5 full questions, selecting one full question from each module.
4. Marks scoredby the student shall be proportionally scaled down to 50 Marks

The theory portion of the IPCC shall be for both CIE and SEE, whereas the practical portion will have a CIE component only. Questions mentioned in the SEE paper may include questions from the practical component.

Suggested Learning Resources:

Text Books

1. Electronic Devices and Circuit Theory, Robert L Boylestad Louis Nashelsky, Pearson, 11th Edition, 2015

2. Electronic Devices and Circuits, Millman and Halkias, Mc Graw Hill, 4th Edition, 2015

3. Electronic Devices and Circuits, David A Bell, Oxford University Press, 5th Edition, 2008

Reference Books

1. Microelectronics CircuitsAnalysis and Design, Muhammad Rashid, Cengage Learning, 2nd Edition, 2014

2. A Text Book of Electrical Technology, Electronic Devices and Circuits, B.L. Theraja, A.K. Theraja, S. Chand, Reprint, 2013
3. Electronic Devices and Circuits, Anil K. Maini, ,VashaAgarval, Wiley, 1st Edition, 2009
4. Electronic Devices and Circuits, S. Salivahanan, Suresh, Mc Graw Hill, 3rd Edition, 2013
5. Fundamentals of Analog Circuits, Thomas L Floyd, Pearson, 2nd Edition, 2012

Web links and Video Lectures (e-Resources):

www.nptel.ac.in

https://www.ti.com/design-resources/design-tools-simulation/analog-circuits/overview.html

https://www.analog.com/en/education/education-library/tutorials/analog-electronics.html

Transformers and Generators			
Course Code	BEE304	CIE Marks	50
Teaching Hours/Week (L:T:P: S)	3:0:0:0	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	03	Exam Hours	03
Examination nature (SEE)	Theory		

Course objectives:

- To understand the construction, working and various tests of single phase Transformer.
- To understand the construction, working and parallel operation of three phase Transformer.
- To understand the construction, working and analysis of Synchronous Generator.
- To understand the construction, working of solar and wind power generators.

Teaching-Learning Process (General Instructions)

These are sample Strategies, which teachers can use to accelerate the attainment of the various course outcomes.

1. Lecturer method (L) needs not to be only traditional lecture method, but alternative effective teaching methods could be adopted to attain the outcomes.
2. Use of Video/Animation to explain functioning of various concepts.
3. Encourage collaborative (Group Learning) Learning in the class.
4. Ask at least three HOT (Higher order Thinking) questions in the class, which promotes critical thinking.
5. Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop design thinking skills such as the ability to design, evaluate, generalize, and analyze information rather than simply recall it.
6. Introduce Topics in manifold representations.
7. Show the different ways to solve the same problem with different circuits/logic and encourage the students to come up with their own creative ways to solve them.
8. Discuss how every concept can be applied to the real world-and when that's possible, it helps improve the students' understanding.

Module-1

Single phase Transformers:

Necessity of transformer, principle of operation, Types and construction, EMF equation, equivalent circuit, Operation of practical transformer under no-load and on-load with phasor diagrams. Losses and methods of reducing losses, efficiency and condition for maximum efficiency. Polarity test, Sumpner's test.

Open circuit and Short circuit tests, calculation of equivalent circuit parameters. Predetermination of efficiency, voltage regulation and its significance. Numerical.

Module-2

Three-phase Transformers: Introduction, Constructional features of three-phase transformers. Transformer connection for three phase operation– star/star, delta/delta and star/delta, comparative features. Labelling of three-phase transformer terminals.

Parallel Operation of Transformers: Necessity of Parallel operation, conditions for parallel operation– Single phase and three phase. Load sharing in case of similar and dissimilar transformers. Numerical.

Auto transformers and Tap changing transformers: Introduction to autotransformer-copper economy, equivalent circuit, no load and on load tap changing transformers. Numerical.

Module-3

Synchronous Generators: Construction, working, Armature windings, winding factors, EMF equation. Harmonics–causes, reduction and elimination. Armature reaction, Synchronous reactance, Equivalent circuit.

Synchronous Generators Analysis: Open circuit and short circuit characteristics, Assessment of reactance-short circuit ratio, Alternator on load. Voltage regulation. Voltage regulation by EMF and MMF methods. Excitation control for constant terminal voltage. Numerical.

Module-4

Synchronous Generators (Salient Pole): Effects of saliency, two-reaction theory, Parallel operation of generators and load sharing. Methods of Synchronization, Synchronizing power.
Performance of Synchronous Generators: Power angle characteristic (salient and non salient pole), power angle diagram, reluctance power, Capability curve for large turbo generators. Hunting and damper windings. Numerical.

Module-5

Wind power Generator –Basic components of wind energy conversion system, types of wind generators- Horizontal and vertical axis. Advantages and disadvantages of WECS.
Solar power generator - principle of solar cell, Basic Solar Photo voltaic, system for power generation, Advantages and disadvantages.

Course outcome (Course Skill Set)

At the end of the course, the student will be able to :

1. Explain the construction, working and various tests of single phase Transformer.
2. Explain the construction, working and parallel operation of three phase Transformer.
3. Explain the construction, working and analysis of Synchronous Generator.
4. Explain the construction, working of solar and wind power generators.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

- For the Assignment component of the CIE, there are 25 marks and for the Internal Assessment Test component, there are 25 marks.
- The first test will be administered after 40-50% of the syllabus has been covered, and the second test will be administered after 85-90% of the syllabus has been covered
- Any two assignment methods mentioned in the 22OB2.4, if an assignment is project-based then only one assignment for the course shall be planned. The teacher should not conduct two assignments at the end of the semester if two assignments are planned.
- For the course, CIE marks will be based on a scaled-down sum of two tests and other methods of assessment.

Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester-End Examination:

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (**duration 03 hours).**

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
3. The students have to answer 5 full questions, selecting one full question from each module.
4. Marks scored sha ll be proportionally reduced to 50 marks

Suggested Learning Resources:

Textbooks

1. Electric Machines, D. P. Kothari, et al, 4th Edition, 2011.
2. Electric Machines, Ashfaq Hussain, Dhanpat Rai & Co, 2nd Edition, 2013.
3. Non conventional Energy sources by G D Rai

Reference Books

1. Electric Machines, Mulukuntla S. Sarma, at el, Cengage, 1st Edition, 2009.
2. Electrical Machines, Drives and Power systems, Theodore Wildi, Pearson, 6th Edition, 2014.
3. Principals of Electrical Machines, V.K Mehta, Rohit Mehta, S Chand, 2nd edition, 2009

Web links and Video Lectures (e-Resources):

- www.nptel.ac.in

Template for Practical Course and if AEC is a practical Course

Transformers and Generators Lab		Semester	III
Course Code	BEEL305	CIE Marks	50
Teaching Hours/Week (L:T:P: S)	0:0:2	SEE Marks	50
Credits	01	Total Marks	100
		Exam Hours	03
Examination nature (SEE)	Practical		

Course objectives:

- To conduct various tests on transformers and synchronous machines and evaluate their performance.
- To perform the parallel operation on two single phase transformers.
- To study and verify the performance of synchronous generator.
- To calculate the voltage regulation of an alternator using different methods for comparison.

Sl.NO	Experiments
1	Open Circuit and Short circuit tests on single phase step up or step down transformer and pre- determination of (i) Efficiency and regulation (ii) Calculation of parameters for equivalent circuit.
2	Sumpner's test on similar transformers and determination of combined and individual transformer efficiency.
3	Parallel operation of two dissimilar single-phase transformers of different kVA and determination of load.
4	Polarity test and connection of 3 single-phase transformers in star – delta and determination of efficiency and regulation under balanced resistive load.
5	Comparison of performance of 3 single-phase transformers in delta – delta and V – V (open delta) connection under load.
6	Separation of hysteresis and eddy current losses in single phase transformer.
7	Investigate the voltage and current ratios of a multi-tapped transformer and verify the ideal transformer ratio.
8	Voltage regulation of an alternator by EMF and MMF methods.
9	Power angle curve of synchronous generator or Direct load test on three phase synchronous generator to determine efficiency and regulation.
10	Performance of synchronous generator connected to infinite bus, under constant power and variable excitation & vice - versa.
11	Model transformer in Simscape for Automatic Voltage Regulation.
12	Simulate power angle curve of generator in MATLAB.

Course outcomes (Course Skill Set):

At the end of the course the student will be able to:

1. Conduct various tests on transformers and synchronous machines and evaluate their performance.
2. Perform the parallel operation on two single phase transformers.
3. Verify the performance of synchronous generator.
4. Calculate the voltage regulation of an alternator using different methods for comparison.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together

Continuous Internal Evaluation (CIE):

CIE marks for the practical course are**50 Marks**.

The split-up of CIE marks for record/ journal and test are in the ratio **60:40**.

- Each experiment is to be evaluated for conduction with an observation sheet and record write-up. Rubrics for the evaluation of the journal/write-up for hardware/software experiments are designed by the faculty who is handling the laboratory session and are made known to students at the beginning of the practical session.
- Record should contain all the specified experiments in the syllabus and each experiment write-up will be evaluated for 10 marks.
- Total marks scored by the students are scaled down to **30 marks** (60% of maximum marks).
- Weightage to be given for neatness and submission of record/write-up on time.
- Department shall conduct a test of 100 marks after the completion of all the experiments listed in the syllabus.
- In a test, test write-up, conduction of experiment, acceptable result, and procedural knowledge will carry a weightage of 60% and the rest 40% for viva-voce.
- The suitable rubrics can be designed to evaluate each student's performance and learning ability.
- The marks scored shall be scaled down to **20 marks** (40% of the maximum marks).

The Sum of scaled-down marks scored in the report write-up/journal and marks of a test is the total CIE marks scored by the student.

Semester End Evaluation (SEE):

- SEE marks for the practical course are 50 Marks.
- SEE shall be conducted jointly by the two examiners of the same institute, examiners are appointed by the Head of the Institute.
- The examination schedule and names of examiners are informed to the university before the conduction of the examination. These practical examinations are to be conducted between the schedule mentioned in the academic calendar of the University.
- All laboratory experiments are to be included for practical examination.
- (Rubrics) Breakup of marks and the instructions printed on the cover page of the answer script to be strictly adhered to by the examiners. **OR** based on the course requirement evaluation rubrics shall be decided jointly by examiners.

- Students can pick one question (experiment) from the questions lot prepared by the examiners jointly.
- Evaluation of test write-up/ conduction procedure and result/viva will be conducted jointly by examiners.

General rubrics suggested for SEE are mentioned here, writeup-20%, Conduction procedure and result in -60%, Viva-voce 20% of maximum marks. SEE for practical shall be evaluated for 100 marks and scored marks shall be scaled down to 50 marks (however, based on course type, rubrics shall be decided by the examiners)

Change of experiment is allowed only once and 15% of Marks allotted to the procedure part are to be made zero.

The minimum duration of SEE is 02 hours

Suggested Learning Resources:

- www.nptel.ac.in

DIGITAL LOGIC CIRCUITS		Semester	III
Course Code	**BEE 306A**	CIE Marks	50
Teaching Hours/Week (L:T:P: S)	3:0:0:0	SEE Marks	50
Total Hours of Pedagogy	40 hours Theory	Total Marks	100
Credits	04	Exam Hours	03
Examination nature (SEE)	Theory		

Course objectives:

- To illustrate simplification of algebraic equations using Karnaugh Maps and Quine-McClusky methods
- To design decoders, encoders, digital multiplexer, adders, subtractors and binary comparators
- To explain latches and flip-flops , registers and counters
- To analyze Melay ad Moore Models
- To develop state diagrams synchronous sequential circuits
- To understand the applications of sequential circuits

Teaching-Learning Process (General Instructions)

These are sample Strategies; that teachers can use to accelerate the attainment of the various course outcomes.

1. Lecturer method (L) needs not to be only traditional lecture method, but alternative effective teaching methods could be adopted to attain the outcomes.
2. Use of Video/Animation to explain functioning of various concepts.
3. Encourage collaborative (Group Learning) Learning in the class.
4. Ask at least three HOT (Higher order Thinking) questions in the class, which promotes critical thinking.
5. Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop design thinking skills such as the ability to design, evaluate, generalize, and analyze information rather than simply recall it.
6. Introduce Topics in manifold representations.
7. Show the different ways to solve the same problem with different circuits/logic and encourage the students to come up with their own creative ways to solve them.
8. Discuss how every concept can be applied to the real world-and when that's possible, it helps improve the students' understanding.

MODULE-1

Principles of Combinational Logic: Definition of combinational logic, canonical forms, Generation of switching equations from truth tables, Karnaugh maps-3,4,5 variables, Incompletely specified functions (Don‘t care terms) Simplifying Max term equations, Quine-McCluskey minimization technique, Quine-McCluskey using don‘t care terms, Reduced prime implicants Tables.

MODULE-2

Analysis and Design of Combinational logic: General approach to combinational logic design, Decoders, BCD decoders, Encoders, digital multiplexers, Using multiplexers as Boolean function generators, Adders and subtractors, Cascading full adders, Look ahead carry, Binary comparators.

MODULE-3

Flip-Flops: Basic Bistable elements, Latches, Timing considerations, The master-slave flip-flops (pulse triggered flip-flops): SR flip-flops, JK flip-flops, Edge triggered flip- flops, Characteristic equations.

MODULE-4

Flip-Flops Applications: Registers, binary ripple counters, synchronous binary counters, Counters based on shift registers, Design of a synchronous counter, Design of a synchronous mod-n counter using clocked T, JK, D and SR flip-flops.

MODULE-5

Sequential Circuit Design: Mealy and Moore models, State machine notation, Synchronous Sequential circuit analysis, Construction of state diagrams, counter design. Memories: Read only and Read/Write Memories, Programmable ROM, EPROM, Flash memory.

Course outcomes (Course Skill Set):

At the end of the course, the student will be able to:

- Explain the concept of combinational and sequential logic circuits
- Analyse and design combinational circuits
- Describe and characterize flip flops and its applications
- Design the sequential circuits using SR, JK, D and T flip-flops and Melay and Moore applications
- Design applications of combinational and sequential circuits
- Employ the digital circuits for different applications

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

- For the Assignment component of the CIE, there are 25 marks and for the Internal Assessment Test component, there are 25 marks.
- The first test will be administered after 40-50% of the syllabus has been covered, and the second test will be administered after 85-90% of the syllabus has been covered
- Any two assignment methods mentioned in the 22OB2.4, if an assignment is project-based then only one assignment for the course shall be planned. The teacher should not conduct two assignments at the end of the semester if two assignments are planned.
- For the course, CIE marks will be based on a scaled-down sum of two tests and other methods of assessment.

Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester-End Examination:

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (**duration 03 hours).**

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
3. The students have to answer 5 full questions, selecting one full question from each module.

Marks scored sha ll be proportionally reduced to 50 marks

Suggested Learning Resources:

Books

1) John M Yarbrough , Digital logic applications and design, Thomson Learning, 2001.

2)Donald D Givone, Digital Principles and design, MC Graw Hill 2002

3)Charles H Roth Jr, Larry L Kinney, Fundamentals of logic design , Cengage Learning, 7th Edition

Reference books:

1)D.P.Kothari and J S Dhillon, -Digital circuits and design, Pearson, 2016

2)Morris Mano, Digital Design, PHI, 3rd edition

3)K.A. Navas, Electronics Lab Manual, Vol.1, PHI 5th edition, 2015.

Web links and Video Lectures (e-Resources):

- https://onlinecourses.nptel.ac.in/noc20_ee32/preview
- YouTube videos on digital electronics
- National Instruments: https://education.ni.com/teach/resources/1104/digital-electronics

Activity Based Learning (Suggested Activities in Class)/ Practical Based learning

- To develop mini projects on digital electronics
- Simple applications like Smart Digital School Bell With Timetable Display, Stop and Go Queue Entry Manager System, Digital Car Turning and Braking Indicator, Digital Nameplate with Visitor Sensing, electronic watch dog etc
- Applications based on PLAs, FPGA, CPLD etc

Electrical Measurements and Instrumentation		Semester	III
Course Code	BEE306B	CIE Marks	50
Teaching Hours/Week (L: T:P: S)	3:0:0:0	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	03	Exam Hours	03
Examination nature (SEE)	Theory		

Course objectives:

- To understand the significance and methods of Measurements, elements of generalised measurement system and errors in measurements.
- To measure resistance, inductance, capacitance by use of different bridges.
- To study the construction, working and characteristics of various instrument transformers.
- To have the working knowledge of electronic instruments and display devices.

Teaching-Learning Process (General Instructions)

These are sample Strategies, which teachers can use to accelerate the attainment of the various course outcomes.

1. Lecturer method (L) needs not to be only traditional lecture method, but alternative effective teaching methods could be adopted to attain the outcomes.
2. Use of Video/Animation to explain functioning of various concepts.
3. Encourage collaborative (Group Learning) Learning in the class.
4. Ask at least three HOT (Higher order Thinking) questions in the class, which promotes critical thinking.
5. Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop design thinking skills such as the ability to design, evaluate, generalize, and analyze information rather than simply recall it.
6. Introduce Topics in manifold representations.
7. Show the different ways to solve the same problem with different circuits/logic and encourage the students to come up with their own creative ways to solve them.
8. Discuss how every concept can be applied to the real world-and when that's possible, it helps improve the students' understanding.

Module-1

Measurements and Measurement systems: Introduction, significance and methods of Measurements, Instruments and measurement systems, Mechanical, electrical and electronic instruments. Classification of instruments. Functions and applications of Measurement systems. Types of Instrumentation systems, information and signal processing. Elements of generalised measurement system. Input-output configurations of measuring instruments and measurement systems. Methods of correction for interfering and modifying inputs, errors in measurements, Accuracy and precision.

Module-2

Measurement of Resistance: Wheatstone's bridge, sensitivity, limitations. Kelvin's double bridge. Earth resistance measurement by fall of potential method and by using Megger.

Measurement of Inductance and Capacitance: Sources and detectors, Maxwell's inductance and capacitance bridge, Hay's bridge, Anderson's bridge, Desauty's bridge, Schering bridge. Shielding of bridges. (Derivations and Numerical as applicable).

Module-3

Instrument Transformers: Introduction, Use of Instrument transformers. Burden on Instrument transformer.

Current transformer (CT): Relationships in CT, Errors in CT, characteristics of CT, causes and reduction of errors in CT, Construction and theory of CT.

Potential transformer (PT): Difference between CT and PT, Relationships in PT, Errors in PT,

characteristics of PT, reduction of errors in PT.

Magnetic measurements: Introduction, measurement of flux/ flux density, magnetising force and leakage factor.

Module-4

Electronic and Digital Instruments: Introduction. Essentials of electronic instruments, Advantages of electronic instruments. True RMS reading voltmeter. Electronic multimeters. Digital voltmeters (DVM) - Ramp type DVM, Integrating type DVM and Successive - approximation DVM. Q meter. Principle of working of electronic energy meter (with block diagram), extra features offered by present day meters and their significance in billing.

Module-5

Display Devices: Introduction, character formats, segment displays, Dot matrix displays, Bar graph displays. Cathode ray tubes, Light emitting diodes, Liquid crystal displays, Nixes, Incandescent, Fluorescent, Liquid vapour and Visual displays.

Recording Devices: Introduction, Strip chart recorders, Galvanometer recorders, Null balance recorders, Potentiometer type recorders, Bridge type recorders, LVDT type recorders, Circular chart and xy recorders. Digital tape recording, Ultraviolet recorders. Electro Cardio Graph (ECG).

Course outcome (Course Skill Set)

At the end of the course, the student will be able to :

1. Explain the significance and methods of Measurements, elements of generalised measurement system and errors in measurements.
2. Measure resistance, inductance and capacitance by different methods.
3. Explain the construction, working and characteristics of various instrument transformers.
4. Explain the working of different electronic instruments and display devices.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

- For the Assignment component of the CIE, there are 25 marks and for the Internal Assessment Test component, there are 25 marks.
- The first test will be administered after 40-50% of the syllabus has been covered, and the second test will be administered after 85-90% of the syllabus has been covered
- Any two assignment methods mentioned in the 22OB2.4, if an assignment is project-based then only one assignment for the course shall be planned. The teacher should not conduct two assignments at the end of the semester if two assignments are planned.
- For the course, CIE marks will be based on a scaled-down sum of two tests and other methods of assessment.

Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester-End Examination:

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (**duration 03 hours).**

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
3. The students have to answer 5 full questions, selecting one full question from each module.
4. Marks scored shall be proportionally reduced to 50 marks

Suggested Learning Resources:

Text Books

1. Electrical and Electronic Measurements and Instrumentation, A.K. Sawhney, Dhanpat Rai & Co, 10th Edition
2. A Course in Electronics and Electrical Measurements and Instrumentation, J. B. Gupta, Katson Books, 2013

Reference Books

1. Electrical and Electronic Measurements and Instrumentation, R.K. Rajput, S Chand, 5th Edition, 2012
2. Electrical Measuring Instruments and Measurements, S.C. Bhargava, BS Publications, 2013
3. Modern Electronic Instrumentation and Measuring Techniques, Cooper D and A.D. Heifrick, Pearson, First Edition, 2015
4. Electronic Instrumentation and Measurements, David A Bell, Oxford University, 3rd Edition, 2013
5. Electronic Instrumentation, H.S.Kalsi, Mc Graw Hill, 3rd Edition,2010

Web links and Video Lectures (e-Resources):

- www.nptel.ac.in
- https://www.eeweb.com/

ELECTROMAGNETIC FIELD THEORY		Semester	III
Course Code	**BEE 306C**	CIE Marks	50
Teaching Hours/Week (L:T:P: S)	3:0:0:0	SEE Marks	50
Total Hours of Pedagogy	40 hours Theory	Total Marks	100
Credits	03	Exam Hours	03
Examination nature (SEE)	Theory		

Course objectives:

- To understand Scalars, Vectors, Cartesian co-ordinate system, relation between different coordinate systems, Coulomb's law, Electric field intensity and its evaluation for different charge conditions.
- To understand potential field of a point charge, Potential gradient, Energy density in the electrostatic field and conductor's properties and boundary conditions.
- To understand Poisson's and Laplace Equations, Biot - Savart's law, Ampere's circuital law and Stokes theorem.
- To understand Magnetic force, Force between differential current elements. Force and torque on a closed circuit, Nature of magnetic materials and Magnetic boundary conditions.
- To understand Faraday's law, Displacement current. Maxwell's equations, Wave propagation in free space and in dielectrics.

Teaching-Learning Process (General Instructions)

These are sample Strategies; that teachers can use to accelerate the attainment of the various course outcomes.

1. Lecturer method (L) needs not to be only traditional lecture method, but alternative effective teaching methods could be adopted to attain the outcomes.
2. Use of Video/Animation to explain functioning of various concepts.
3. Encourage collaborative (Group Learning) Learning in the class.
4. Ask at least three HOT (Higher order Thinking) questions in the class, which promotes critical thinking.
5. Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop design thinking skills such as the ability to design, evaluate, generalize, and analyze information rather than simply recall it.
6. Introduce Topics in manifold representations.
7. Show the different ways to solve the same problem with different circuits/logic and encourage the students to come up with their own creative ways to solve them.
8. Discuss how every concept can be applied to the real world-and when that's possible, it helps improve the students' understanding.

MODULE-1

Vector Analysis:

Scalars and Vectors, Vector algebra, Cartesian co-ordinate system, Vector Components and unit vectors. Scalar field and Vector field. Dot product and Cross product, Gradient of a scalar field. Divergence and Curl of a vector field. Co – ordinate systems: cylindrical and spherical, relation between different coordinate systems. Expression for gradient, divergence and curl in rectangular, cylindrical and spherical co-ordinate systems. Numerical.

Electrostatics:

Coulomb's law, Electric field intensity and its evaluation for (i) point charge (ii) line charge (iii) surface charge (iv) volume charge distributions. Electric flux density, Gauss law and its applications. Maxwell's first equation (Electrostatics). Divergence theorem. Numerical.

MODULE-2

Energy and Potential:

Energy expended in moving a point charge in an electric field. The line integral. Definition of potential difference and potential. The potential field of a point charge and of a system of charges. Potential gradient. The dipole. Energy density in the electrostatic field. Numerical.

Conductor and Dielectrics:

Current and current density. Continuity of current. Metallic conductors, conductor's properties and boundary conditions. Perfect dielectric materials, capacitance calculations. Parallel plate capacitor with two dielectrics with dielectric interface parallel to the conducting plates. Numerical.

MODULE-3
Poisson's and Laplace Equations: Derivations and problems, Uniqueness theorem. **Steady magnetic fields:** Biot - Savart's law, Ampere's circuital law. The Curl. Stokes theorem. Magnetic flux and flux density. Scalar and vector magnetic potentials. Numerical.
MODULE-4
Magnetic forces: Force on a moving charge and differential current element. Force between differential current elements. Force and torque on a closed circuit. Numerical. **Magnetic Materials and Magnetism:** Nature of magnetic materials, magnetisation and permeability. Magnetic boundary conditions. Magnetic circuit, inductance and mutual inductance. Numerical.
MODULE-5
Time Varying Fields and Maxwell's Equations: Faraday's law, Displacement current. Maxwell's equations in point form and integral form. Numerical. **Uniform plane wave:** Electromagnetic radiation: near field—non-radiative and radiative, far field. Wave propagation in free space and in dielectrics. Pointing vector and power considerations. Propagation in good conductors, skin effect. Numerical.

Course outcomes (Course Skill Set):

At the end of the course, the student will be able to:

- Explain Scalars, Vectors, Cartesian co-ordinate system, relation between different coordinate systems, Coulomb's law, Electric field intensity and its evaluation for different charge conditions.
- Explain the potential field of a point charge, Potential gradient, Energy density in the electrostatic field and conductor's properties and boundary conditions.
- Explain the Poisson's and Laplace Equations, Biot - Savart's law, Ampere's circuital law and Stokes theorem.
- Explain the Magnetic force, Force between differential current elements. Force and torque on a closed circuit, Nature of magnetic materials and Magnetic boundary conditions.
- Explain the Faraday's law, Displacement current. Maxwell's equations, Wave propagation in free space and in dielectrics.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

- For the Assignment component of the CIE, there are 25 marks and for the Internal Assessment Test component, there are 25 marks.
- The first test will be administered after 40-50% of the syllabus has been covered, and the second test will be administered after 85-90% of the syllabus has been covered
- Any two assignment methods mentioned in the 22OB2.4, if an assignment is project-based then only one assignment for the course shall be planned. The teacher should not conduct two assignments at the end of the semester if two assignments are planned.
- For the course, CIE marks will be based on a scaled-down sum of two tests and other methods of assessment.

Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester-End Examination:

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (**duration 03 hours).**

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
3. The students have to answer 5 full questions, selecting one full question from each module.
4. Marks scored shall be proportionally reduced to 50 marks

Suggested Learning Resources:

Books

1 Engineering Electromagnetics William H Hayt et al McGraw Hill 8thEdition, 2014
2 Principles of Electromagnetics Matthew N. O. Sadiku Oxford 6th Edition, 2015

Reference books:

1 Fundamentals of Engineering Electromagnetics David K. Cheng Pearson 2014
2 Electromagnetism -Theory (Volume -1) -Applications (Volume-2) Ashutosh Pramanik PHI Learning 2014
3 Electromagnetic Field Theory Fundamentals Bhag Guru et al Cambridge 2005
4 Electromagnetic Field Theory RohitKhurana Vikas Publishing 1st Edition,2014

Web links and Video Lectures (e-Resources):

- YouTube videos
- www.nptel.ac.in

PHYSICS OF ELECTRONIC DEVICES		Semester	III
Course Code	**BEE306D**	CIE Marks	50
Teaching Hours/Week (L:T:P: S)	3:0:0:0	SEE Marks	50
Total Hours of Pedagogy	40 Hours Theory	Total Marks	100
Credits	03	Exam Hours	03
Examination nature (SEE)	Theory		

Course objectives:

This course will enable students to

- Understand the basics of semiconductor physics and electronic devices
- Describe the mathematical models BGTs and FETs along with the constructional details
- Understand the construction and working principles of optoelectronic devices
- Understand the fabrication process of semiconductor devices and CMOS process integration

Teaching-Learning Process (General Instructions)

These are sample Strategies, which teachers can use to accelerate the attainment of the various course outcomes.

1. Lecturer method (L) needs not to be only traditional lecture method, but alternative effective teaching methods could be adopted to attain the outcomes.
2. Use of Video/Animation to explain functioning of various concepts.
3. Encourage collaborative (Group Learning) Learning in the class.
4. Ask at least three HOT (Higher order Thinking) questions in the class, which promotes critical thinking.
5. Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop design thinking skills such as the ability to design, evaluate, generalize, and analyze information rather than simply recall it.
6. Introduce Topics in manifold representations.
7. Show the different ways to solve the same problem with different circuits/logic and encourage the students to come up with their own creative ways to solve them.
8. Discuss how every concept can be applied to the real world-and when that's possible, it helps improve the students' understanding.

Module-1

Semiconductors

Bonding forces in solids, energy bands, metals, semiconductors and insulators, direct and indirect semiconductors, electrons and holes, intrinsic and extrinsic materials, conductivity and mobility, drift and resistance, effects of temperature and doping on mobility, Hall effect

Text:1) 3.1.1 to 3.1.4, 3.2.1 to 3.2.4, 3.4.1 to 3.4.5

Module-2

P-N JUNCTIONS:

Forward and reverse bias junctions, Qualitative description of current flow at a junction, reverse bias and reverse bias breakdown, Zener breakdown, avalanche breakdown, Thermal runaway.

Text 1)5.3.1 to 5.3.3, 5.4, 5.4.1 to 5.4.3

Optoelectronic Devices:

Photo diodes, current and voltage in illuminated junction, solar cells, photo detectors, light emitting diode, light emitting materials

Text 1)8.1.1 to 8.1.3, 8.2, 8.2.1

Module-3

Bipolar Junction Transistor:

Fundamentals of BJT operation, amplification with BJTs, BJT fabrication, the Coupled diode model (Ebers –Moll Model), switching operation of transistor, cutoff, saturation, switching cycle, specifications, drift in the base region, base narrowing, avalanche breakdown.

Text 1)7.1 to 7.3, 7.5.1, 7.6, 7.7.1 to 7.7.3

Module-4

Field Effect Transistors:

Basic PN JFET operation, equivalent circuit and frequency limitation, MOSFET two terminal MOS structure, energy band diagram, ideal capacitance voltage characteristics and frequency effects, basic MOSFET operation, MOSFET structure, current-voltage characteristics

Text 2)9.1.1, 9.4, 9.6.1 - 9.6.2, 9.7.1-9.7.2, 9.8.1-9.8.2

Module-5

Fabrication of PN junction:

Thermal oxidation, diffusion, rapid thermal processing, Ion implantation, chemical vapour deposition, photolithography, etching, metallization

(Text 1)5.1

Integrated Circuits:

Background, evolution of ICs, CMOS process integration, integration of other circuit elements

(Text 1)9.1-9.2, 9.3.1, 9.3.3.

Course outcome (Course Skill Set)

At the end of the course, the student will be able to :

1. Understand the principles of semiconductor physics
2. Understand the principles and characteristics of different types of semiconductor devices
3. Understand the fabrication process of semiconductor devices
4. Utilize the mathematical models of MOS transistors for circuits and systems
5. Identify the mathematical models of MOS transistors for circuits and systems

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

- For the Assignment component of the CIE, there are 25 marks and for the Internal Assessment Test component, there are 25 marks.
- The first test will be administered after 40-50% of the syllabus has been covered, and the second test will be administered after 85-90% of the syllabus has been covered
- Any two assignment methods mentioned in the 22OB2.4, if an assignment is project-based then only one assignment for the course shall be planned. The teacher should not conduct two assignments at the end of the semester if two assignments are planned.
- For the course, CIE marks will be based on a scaled-down sum of two tests and other methods of assessment.

Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester-End Examination:

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (**duration 03 hours).**

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
3. The students have to answer 5 full questions, selecting one full question from each module.
4. Marks scored shall be proportionally reduced to 50 marks

Suggested Learning Resources:

Text Books:

1)Ben. G. Streetman, Sanjay Kumar Banerjee, "Solid State Electronic Devices", 7th Edition, Pearson Education 2016, ISBN 978-93-325-5508-2

2)Donald A Neamen, Dhrubes Biswas, "Semiconductor physics and Devices", 4th Edition, MC Graw Hill Education 2012, ISBN 978-0-07-107010-2

Reference Books:

1)S.M. Sze, Kwok K Ng, "Physics of semiconductor devices", 3rd edition, Wiley 2018.

2)Adir Bar-Lev, "Semiconductor and electronic devices", 3rd Edition , PHI, 1993.

Web links and Video Lectures (e-Resources):

- NPTEL lecturers on semiconductor physics: https://archive.nptel.ac.in/courses/108/108/108108122/
- Undergraduate course on semiconductor physics ;https://www.udemy.com/course/semiconductor-device-physics-an-introduction/
- You tube videos on semiconductor physics

Activity Based Learning (Suggested Activities in Class)/ Practical Based learning

- Applications of optoelectronics devices
- Applications and basics of microelectronic fabrication

Scilab / MATLAB for Transformers & Generators			
Course Code	**BEEL358A**	CIE Marks	50
Teaching Hours/Week (L:T:P: S)	0:0:2:0	SEE Marks	50
Credits	01	Exam Hours	02

Course objectives:

(1) Along with prescribed hours of teaching –learning process, provide opportunity to perform the experiments/programmes at their own time, at their own pace, at any place as per their convenience and repeat any number of times to understand the concept.

(2) Provide unhindered access to perform whenever the students wish.

(3) Vary different parameters to study the behavior of the circuit without the risk of damaging equipment/device or injuring themselves.

Sl. NO	Experiments
1	Open Circuit and Short circuit tests on single phase step up or step down transformer and predetermination of (i) Efficiency and regulation (ii) Calculation of parameters of equivalent circuit.
2	Sumpner's test on similar transformers and determination of combined and individual transformer efficiency.
3	Parallel operation of two dissimilar single-phase transformers of different kVA and determination of load sharing and analytical verification given the Short circuit test data.
4	Separation of hysteresis and eddy current losses in single phase transformer.
5	Voltage regulation of an alternator by EMF and MMF methods.
6	Voltage regulation of an alternator by ZPF method.
7	Power angle curve of synchronous generator.
8	Slip test – Measurement of direct and quadrature axis reactance and predetermination of regulation of salient pole synchronous machines.

Course outcomes (Course Skill Set):

At the end of the course the student will be able to:

- Analyse in an intelligent manner, think better, and perform better.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each course. The student has to secure not less than 35% (18 Marks out of 50) in the semester-end examination(SEE).

Continuous Internal Evaluation (CIE):

CIE marks for the practical course is **50 Marks**.

The split-up of CIE marks for record/ journal and test are in the ratio **60:40**.

- Each experiment to be evaluated for conduction with observation sheet and record write-up. Rubrics for the evaluation of the journal/write-up for hardware/software experiments designed by the faculty who is handling the laboratory session and is made known to students at the beginning of the practical session.
- Record should contain all the specified experiments in the syllabus and each experiment write-up will be evaluated for 10 marks.
- Total marks scored by the students are scaled downed to 30 marks (60% of maximum marks).
- Weightage to be given for neatness and submission of record/write-up on time.
- Department shall conduct 02 tests for 100 marks, the first test shall be conducted after the 8^{th} week of the semester and the second test shall be conducted after the 14^{th} week of the semester.
- In each test, test write-up, conduction of experiment, acceptable result, and procedural knowledge will carry a weightage of 60% and the rest 40% for viva-voce.
- The suitable rubrics can be designed to evaluate each student's performance and learning ability. Rubrics suggested in Annexure-II of Regulation book
- The average of 02 tests is scaled down to 20 marks (40% of the maximum marks).

The Sum of scaled-down marks scored in the report write-up/journal and average marks of two tests is the total CIE marks scored by the student.

Semester End Evaluation (SEE):

- SEE marks for the practical course is 50 Marks.
- SEE shall be conducted jointly by the two examiners of the same institute, examiners are appointed by the University
- All laboratory experiments are to be included for practical examination.
- (Rubrics) Breakup of marks and the instructions printed on the cover page of the answer script to be strictly adhered to by the examiners. OR based on the course requirement evaluation rubrics shall be decided jointly by examiners.
- Students can pick one question (experiment) from the questions lot prepared by the internal /external examiners jointly.
- Evaluation of test write-up/ conduction procedure and result/viva will be conducted jointly by examiners. General rubrics suggested for SEE are mentioned here, writeup-20%, Conduction procedure and result in - 60%, Viva-voce 20% of maximum marks. SEE for practical shall be evaluated for 100 marks and scored marks shall be scaled down to 50 marks (however, based on course type, rubrics shall be decided by the examiners)
- Change of experiment is allowed only once and 15% Marks allotted to the procedure part to be made zero. The duration of SEE is 03 hours.
- Rubrics suggested in Annexure-II of Regulation book.

555 IC Laboratory			
Course Code	**BEEL358B**	CIE Marks	50
Teaching Hours/Week (L:T:P: S)	0:0:2:0	SEE Marks	50
Credits	01	Exam Hours	02

Course objectives:

(1) Along with prescribed hours of teaching –learning process, provide opportunity to perform the experiments/programmes at their own time, at their own pace, at any place as per their convenience and repeat any number of times to understand the concept.

(2) Provide unhindered access to perform whenever the students wish.

(3) Vary different parameters to study the behaviour of the circuit without the risk of damaging equipment/device or injuring themselves.

Sl. NO	Experiments
1	Construct Astable Multivibrator circuit using IC-555 Timer.
2	Construct Mono-stable Multivibrator circuit using IC-555 Timer.
3	Construct and test Sequential timer using IC-555.
4	Generate Pulse Width Modulator (PWM) signal using IC-555 Timer.
5	Construct Burglar Alarm circuit using IC-555 Timer.
6	Construct and generate Frequency Shift Keying (FSK) signal using IC-555 Timer.
7	Construct and test Running LED circuit using IC-555 Timer.
8	Construct water level indicator using IC-555 Timer.
9	Construct continuity tester using IC-555 Timer.

Course outcomes (Course Skill Set):

At the end of the course the student will be able to:

- Analyse in an intelligent manner, think better, and perform better.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each course. The student has to secure not less than 35% (18 Marks out of 50) in the semester-end examination(SEE).

Continuous Internal Evaluation (CIE):

CIE marks for the practical course is **50 Marks**.

The split-up of CIE marks for record/ journal and test are in the ratio **60:40**.

- Each experiment to be evaluated for conduction with observation sheet and record write-up. Rubrics for the evaluation of the journal/write-up for hardware/software experiments designed by the faculty who is handling the laboratory session and is made known to students at the beginning of the practical session.
- Record should contain all the specified experiments in the syllabus and each experiment write-up will be evaluated for 10 marks.
- Total marks scored by the students are scaled downed to 30 marks (60% of maximum marks).
- Weightage to be given for neatness and submission of record/write-up on time.
- Department shall conduct 02 tests for 100 marks, the first test shall be conducted after the 8th week of the semester and the second test shall be conducted after the 14th week of the semester.
- In each test, test write-up, conduction of experiment, acceptable result, and procedural knowledge will carry a weightage of 60% and the rest 40% for viva-voce.

- The suitable rubrics can be designed to evaluate each student's performance and learning ability. Rubrics suggested in Annexure-II of Regulation book
- The average of 02 tests is scaled down to **20 marks** (40% of the maximum marks).
- The Sum of scaled-down marks scored in the report write-up/journal and average marks of two tests is the totalCIE marks scored by the student.

- **Semester End Evaluation (SEE):**
- SEE marks for the practical course is 50 Marks.
- SEE shall be conducted jointly by the two examiners of the same institute, examiners are appointed by theUniversity
- All laboratory experiments are to be included for practical examination.
- (Rubrics) Breakup of marks and the instructions printed on the cover page of the answer script to be strictly adhered to by the examiners. **OR** based on the course requirement evaluation rubrics shall be decided jointlyby examiners.
- Students can pick one question (experiment) from the questions lot prepared by the internal /external examiners jointly.
- Evaluation of test write-up/ conduction procedure and result/viva will be conducted jointly by examiners. General rubrics suggested for SEE are mentioned here, writeup-20%, Conduction procedure and result in -60%, Viva-voce 20% of maximum marks. SEE for practical shall be evaluated for 100 marks and scored marks shall be scaled down to 50 marks (however, based on course type, rubrics shall be decided by theexaminers)
- Change of experiment is allowed only once and 15% Marks allotted to the procedure part to be made zero.The duration of SEE is 03 hours
- Rubrics suggested in Annexure-II of Regulation book.

Circuit Laboratory using P-spice			
Course Code	**BEEL358C**	CIE Marks	50
Teaching Hours/Week (L:T:P: S)	0:0:2:0	SEE Marks	50
Credits	01	Exam Hours	02

Course objectives:

(1) Along with prescribed hours of teaching –learning process, provide opportunity to perform the experiments/programmes at their own time, at their own pace, at any place as per their convenience and repeat any number of times to understand the concept.

(2) Provide unhindered access to perform whenever the students wish.

(3) Vary different parameters to study the behaviour of the circuit without the risk of damaging equipment/ device or injuring themselves.

Sl. NO	Experiments
1	Simulate Series RL & RC circuit and observe phase difference between waveforms of voltage and current.
2	Simulation and verification of Kirchhoff's Current Law & Kirchhoff's Voltage Law.
3	Simulation of Mesh analysis for a given circuit.
4	Simulation of Nodal analysis for a given circuit.
5	Determination of Z & Y parameters of a given two-port network.
6	Simulate and verify Super Positions theorem.
7	Simulation and verification Reciprocity theorem.
8	Simulation and verification Thevenin's and Norton's theorem.
9	Simulation and verification Maximum Power Transfer theorem.
10	Simulation and verification Millman's theorem.
11	Simulation of Series and Parallel Resonance circuit.

Course outcomes (Course Skill Set):

At the end of the course the student will be able to:

- Analyse in an intelligent manner, think better, and perform better.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each course. The student has to secure not less than 35% (18 Marks out of 50) in the semester-end examination(SEE).

Continuous Internal Evaluation (CIE):

CIE marks for the practical course is **50 Marks**.

The split-up of CIE marks for record/ journal and test are in the ratio **60:40**.

- Each experiment to be evaluated for conduction with observation sheet and record write-up. Rubrics for the evaluation of the journal/write-up for hardware/software experiments designed by the faculty who is handling the laboratory session and is made known to students at the beginning of the practical session.
- Record should contain all the specified experiments in the syllabus and each experiment write-up will be evaluated for 10 marks.
- Total marks scored by the students are scaled downed to 30 marks (60% of maximum marks).
- Weightage to be given for neatness and submission of record/write-up on time.
- Department shall conduct 02 tests for 100 marks, the first test shall be conducted after the 8^{th} week of the semester and the second test shall be conducted after the 14^{th} week of the semester.
- In each test, test write-up, conduction of experiment, acceptable result, and procedural knowledge will carry a weightage of 60% and the rest 40% for viva-voce.

- The suitable rubrics can be designed to evaluate each student's performance and learning ability. Rubrics suggested in Annexure-II of Regulation book
- The average of 02 tests is scaled down to **20 marks** (40% of the maximum marks).

The Sum of scaled-down marks scored in the report write-up/journal and average marks of two tests is the total CIE marks scored by the student.

Semester End Evaluation (SEE):

- SEE marks for the practical course is 50 Marks.
- SEE shall be conducted jointly by the two examiners of the same institute, examiners are appointed by theUniversity
- All laboratory experiments are to be included for practical examination.
- (Rubrics) Breakup of marks and the instructions printed on the cover page of the answer script to be strictly adhered to by the examiners. **OR** based on the course requirement evaluation rubrics shall be decided jointlyby examiners.
- Students can pick one question (experiment) from the questions lot prepared by the internal /external examiners jointly.
- Evaluation of test write-up/ conduction procedure and result/viva will be conducted jointly by examiners. General rubrics suggested for SEE are mentioned here, writeup-20%, Conduction procedure and result in -60%, Viva-voce 20% of maximum marks. SEE for practical shall be evaluated for 100 marks and scoredmarks shall be scaled down to 50 marks (however, based on course type, rubrics shall be decided by theexaminers)
- Change of experiment is allowed only once and 15% Marks allotted to the procedure part to be made zero.The duration of SEE is 03 hours
- Rubrics suggested in Annexure-II of Regulation book.

ELECTRICAL HARDWARE LABORATORY			
Course Code	**BEEL358D**	CIE Marks	50
Teaching Hours/Week (L:T:P: S)	0:0:2:0	SEE Marks	50
Credits	01	Exam Hours	02

Course objectives:

(1) Along with prescribed hours of teaching –learning process, provide opportunity to perform the experiments/programmes at their own time, at their own pace, at any place as per their convenience and repeat any number of times to understand the concept.

(2) Provide unhindered access to perform whenever the students wish.

(3) Vary different parameters to study the behaviour of the circuit without the risk of damaging equipment/device or injuring themselves.

Sl. NO	Experiments
1	Verification of KCL and KVL for DC Circuits.
2	Verification of KCL and KVL for AC Circuits.
3	Measurement of Current, Power and Power Factor of Incandescent Lamp, Fluorescent Lamp and LED Lamp.
4	Evaluate the loading effect of Voltmeter of electric circuits.
5	Measurement of Resistance using V-I method.
6	Measurement of Resistance and Inductance of a Choke coil using three voltmeter method.
7	Determination of Phase and Line quantities in three-phase star and delta connected loads.
8	Two-Way and Three-Way Control of Lamp and Formation of Truth Table.
9	Measurement of Earth Resistance using fall of potential method.
10	Determination of fuse characteristics.

Course outcomes (Course Skill Set):

At the end of the course the student will be able to:

- Analyse in an intelligent manner, think better, and perform better.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each course. The student has to secure not less than 35% (18 Marks out of 50) in the semester-end examination(SEE).

Continuous Internal Evaluation (CIE):

CIE marks for the practical course is **50 Marks**.

The split-up of CIE marks for record/ journal and test are in the ratio **60:40**.

- Each experiment to be evaluated for conduction with observation sheet and record write-up. Rubrics for the evaluation of the journal/write-up for hardware/software experiments designed by the faculty who is handling the laboratory session and is made known to students at the beginning of the practical session.
- Record should contain all the specified experiments in the syllabus and each experiment write-up will be evaluated for 10 marks.
- Total marks scored by the students are scaled downed to 30 marks (60% of maximum marks).
- Weightage to be given for neatness and submission of record/write-up on time.
- Department shall conduct 02 tests for 100 marks, the first test shall be conducted after the 8th week of the semester and the second test shall be conducted after the 14th week of the semester.

- In each test, test write-up, conduction of experiment, acceptable result, and procedural knowledge will carry a weightage of 60% and the rest 40% for viva-voce.
- The suitable rubrics can be designed to evaluate each student's performance and learning ability. Rubrics suggested in Annexure-II of Regulation book
- The average of 02 tests is scaled down to **20 marks** (40% of the maximum marks).
- The Sum of scaled-down marks scored in the report write-up/journal and average marks of two tests is the totalCIE marks scored by the student.

- **Semester End Evaluation (SEE):**
- SEE marks for the practical course is 50 Marks.
- SEE shall be conducted jointly by the two examiners of the same institute, examiners are appointed by theUniversity
- All laboratory experiments are to be included for practical examination.
- (Rubrics) Breakup of marks and the instructions printed on the cover page of the answer script to be strictly adhered to by the examiners. **OR** based on the course requirement evaluation rubrics shall be decided jointlyby examiners.
- Students can pick one question (experiment) from the questions lot prepared by the internal /external examiners jointly.
- Evaluation of test write-up/ conduction procedure and result/viva will be conducted jointly by examiners. General rubrics suggested for SEE are mentioned here, writeup-20%, Conduction procedure and result in -60%, Viva-voce 20% of maximum marks. SEE for practical shall be evaluated for 100 marks and scored marks shall be scaled down to 50 marks (however, based on course type, rubrics shall be decided by theexaminers)
- Change of experiment is allowed only once and 15% Marks allotted to the procedure part to be made zero.The duration of SEE is 03 hours
- Rubrics suggested in Annexure-II of Regulation book.

ELECTRIC MOTORS		Semester	IV
Course Code	BEE401	CIE Marks	50
Teaching Hours/Week (L:T:P: S)	3:0:0:0	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	03	Exam Hours	03
Examination nature (SEE)	Theory		

Course objectives:

1 To study the constructional features of Motors and select a suitable drive for specific Application.
2 To study the constructional features of Three Phase and Single phase induction Motors.
3 To study different test to be conducted for the assessment of the performance characteristics of motors.
4 To study the speed control of motor by a different methods.
5 Explain the construction and operation of Synchronous motor and special motors.

Teaching-Learning Process (General Instructions)

These are sample Strategies, which teachers can use to accelerate the attainment of the various course outcomes.

1. Lecturer method (L) needs not to be only traditional lecture method, but alternative effective teaching methods could be adopted to attain the outcomes.
2. Use of Video/Animation to explain functioning of various concepts.
3. Encourage collaborative (Group Learning) Learning in the class.
4. Ask at least three HOT (Higher order Thinking) questions in the class, which promotes critical thinking.
5. Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop design thinking skills such as the ability to design, evaluate, generalize, and analyse information rather than simply recall it.
6. Introduce Topics in manifold representations.
7. Show the different ways to solve the same problem with different circuits/logic and encourage the students to come up with their own creative ways to solve them.
8. Discuss how every concept can be applied to the real world - and when that's possible, it helps improve the students' understanding.

Module-1

DC Motors: Construction and working principle. Back E.M.F and its significance, Torque equation, Classification, Characteristics of shunt, series & compound motors, Speed control of shunt motor, Application of motors.

Losses and Efficiency- Losses in DC motors, power flow diagram, efficiency, condition for maximum efficiency.

Testing of DC Motors: Direct & indirect methods of testing of DC motors- Swinburne's test, Field's test, merits and demerits of tests. (numerical as applicable)

Module-2

Three Phase Induction Motors: Concept and generation of rotating magnetic field, Principle of operation, construction, classification and types; squirrel-cage, slip-ring. Slip and its significance, Torque equation, torque-slip characteristic covering motoring, generating and braking regions of operation, Maximum torque, (numerical as applicable)

Module-3
Performance of Three-Phase Induction Motor: Phasor diagram of induction motor on no-load and on load, equivalent circuit, losses, efficiency, No-load and blocked rotor tests. Performance of the motor from the equivalent circuit. Cogging and crawling. High torque rotors-double cage and deep rotor bars. Induction motor working as induction generator, construction and working of doubly fed induction generator. (numerical as applicable)
Module-4
Starting and Speed Control of Three-Phase Induction Motors: Necessity of starter. Direct on line, Star-Delta, and autotransformer starting. Rotor resistance starting. Speed control by frequency. **Single-Phase Induction Motor:** Double revolving field theory and principle of operation. Construction and operation of split-phase, capacitor start and capacitor run and shaded pole motors. Comparison of single phase motors and applications. (numerical as applicable)
Module-5
Synchronous Motor: Principle of operation, phasor diagrams, torque and torque angle, effect of change in load, effect of change in excitation. V and inverted V curves. Synchronous condenser, **Other Motors:** Construction and operation of Universal motor, AC servomotor, Linear induction motor, PMSM, SRM and BLDC.
Course outcome (Course Skill Set) At the end of the course, the student will be able to : 1 Understand the construction and operation, characteristics, Testing of DC Motors and determine losses and efficiency. 2 Understand the construction and operation, classification and types of Three phase Induction motors. 3 Describe the performance characteristics and applications of three phase Induction motors. 4 Demonstrate and explain Speed Control methods of three phase induction motor and types of single phase induction motors. 5 Understand the construction and operation, V and inverted V curves of synchronous motors. 6 Construction and operation of Universal motor, AC servomotor, Linear induction motor, PMSM, SRM and BLDC motors.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

- For the Assignment component of the CIE, there are 25 marks and for the Internal Assessment Test component, there are 25 marks.
- The first test will be administered after 40-50% of the syllabus has been covered, and the second test will be administered after 85-90% of the syllabus has been covered
- Any two assignment methods mentioned in the 22OB2.4, if an assignment is project-based then only one assignment for the course shall be planned. The teacher should not conduct two assignments at the end of the semester if two assignments are planned.
- For the course, CIE marks will be based on a scaled-down sum of two tests and other methods of assessment.

Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester-End Examination:

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (**duration 03 hours).**

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.

Suggested Learning Resources:

Text Books

1. Electric Machines, D. P. Kothari, I. J. Nagrath, McGraw Hill, 4th edition, 2011.
2. Theory of Alternating Current Machines, Alexander Langsdorf, McGraw Hill, 2nd Edition, 2001.
3. Electric Machines, AshfaqHussain, DhanpatRai& Co, 2nd Edition, 2013.

Reference Books

1. Electrical Machines, Drives and Power systems, Theodore Wildi, Pearson, 6th Edition, 2014
2. Electrical Machines, M.V. Deshpande, PHI Learning, 2013
3. Electric Machinery and Transformers, Bhag S. Guru at el, Oxford University Press, 3rd Edition, 2012
4. Electric Machinery and Transformers, Irving Kosow, Pearson, 2nd Edition, 2012
5. Principles of Electric Machines and power Electronic, P.C.Sen, Wiley, 2nd Edition, 2013
6. Electrical Machines, R.K. Srivastava, Cengage Learning, 2nd Edition, 2013

Web links and Video Lectures (e-Resources):
• https://nptel.ac.in • http:// acl.digimat.in/nptel/courses/video/108105017/108105017.html
Activity Based Learning (Suggested Activities in Class)/ Practical Based learning • Quizzes. • Seminars. • Cut sectional view of ac and dc motors • Animated/NPTEL videos • PPTs

Transmission and Distribution		Semester	IV
Course Code	BEE402	CIE Marks	50
Teaching Hours/Week (L: T:P: S)	4:0:0	SEE Marks	50
Total Hours of Pedagogy	50 Hours	Total Marks	100
Credits	04	Exam Hours	03
Examination nature (SEE)	Theory		

Course objectives:

- To understand the structure of electrical power system, its components, advantages of high voltage AC and DC transmission, various conductors used for transmission, sag and its calculation.
- To understand various types of insulators, methods to improve string efficiency.
- To understand the various transmission line parameters, their effects on transmission of electricity.
- To understand the various parameters that influences the performance of transmission line and to calculate performance parameters of various transmission lines.
- To understand carona and its effects, underground cables, its construction, classification, limitations and specifications.
- To understand and evaluate different types of distribution systems.

Teaching-Learning Process (General Instructions)

These are sample Strategies, which teachers can use to accelerate the attainment of the various course outcomes.

1. Lecturer method (L) needs not to be only traditional lecture method, but alternative effective teaching methods could be adopted to attain the outcomes.
2. Use of Video/Animation to explain functioning of various concepts.
3. Encourage collaborative (Group Learning) Learning in the class.
4. Ask at least three HOT (Higher order Thinking) questions in the class, which promotes critical thinking.
5. Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop design thinking skills such as the ability to design, evaluate, generalize, and analyze information rather than simply recall it.
6. Introduce Topics in manifold representations.
7. Show the different ways to solve the same problem with different circuits/logic and encourage the students to come up with their own creative ways to solve them.
8. Discuss how every concept can be applied to the real world-and when that's possible, it helps improve the students' understanding.

Module-1

Introduction to Power System: Structure of electric power system: generation, transmission and distribution. Advantages of higher voltage transmission: HVAC, EHVAC, UHVAC and HVDC. Interconnection. Feeders, distributors and service mains.

Overhead Transmission Lines: A brief introduction to types of supporting structures and line conductors- Conventional conductors; Aluminium Conductor steel reinforced (ACSR), All – aluminium alloy conductor (AAAC) and All –aluminium conductor (AAC). High temperature conductors; Thermal resistant aluminium alloy (ATI),Super thermal resistant aluminium alloy (ZTAI), Gap type thermal resistant aluminium alloy conductor steel reinforced (GTACSR), Gap type super thermal resistant aluminium alloy conductor steel reinforced (GZTACSR). Bundle conductor and its advantages. Importance of sag, Sag calculation – supports at same and different levels, effect of wind and ice. Line vibration and vibration dampers. Overhead line protection against lightening; ground wires.

Overhead Line Insulators: A brief introduction to types of insulators, material used- porcelain, toughened glass and polymer (composite). Potential distribution over a string of suspension insulators. String efficiency, Methods of increasing string efficiency. Arcing horns.

Module-2
Line Parameters: Introduction to line parameters- resistance, inductance and capacitance. Calculation of inductance of single phase and three phase lines with equilateral spacing, unsymmetrical spacing, double circuit and transposed lines. Inductance of composite – conductors, geometric mean radius (GMR) and geometric mean distance (GMD). Calculation of capacitance of single phase and three phase lines with equilateral spacing, unsymmetrical spacing, double circuit and transposed lines. Capacitance of composite – conductor, geometric mean radius (GMR) and geometric mean distance (GMD). Advantages of single circuit and double circuit lines.
Module-3
Performance of Transmission Lines: Classification of lines – short, medium and long. Current and voltage relations, line regulation and Ferranti effect in short length lines, medium length lines considering Nominal T and nominal circuits, and long lines considering hyperbolic form equations. Equivalent circuit of a long line. ABCD constants in all cases.
Module-4
Corona: Phenomena, disruptive and visual critical voltages, corona loss. Advantages and disadvantages of corona. Methods of reducing corona. **Underground Cable:** Types of cables, constructional features, insulation resistance, thermal rating, charging current, grading of cables – capacitance and inter-sheath. Dielectric loss. Comparison between ac and DC cables. Limitations of cables. Specification of power cables.
Module-5
Distribution: Primary AC distribution systems – Radial feeders, parallel feeders, loop feeders and interconnected network system. Secondary AC distribution systems – Three phase 4 wire system and single phase 2 wire distribution, AC distributors with concentrated loads. Effect of disconnection of neutral in a 3 phase four wire system. **Reliability and Quality of Distribution System:** Introduction, definition of reliability, failure, probability concepts, limitation of distribution systems, power quality, Reliability aids.

Course outcome (Course Skill Set)

At the end of the course, the student will be able to :

1. Explain the structure of electrical power system, its components, advantages of high voltage AC and DC transmission, various conductors used for transmission, sag and its calculation.
2. Explain various types of insulators and methods to improve string efficiency.
3. Explain the various transmission line parameters, their effects on transmission of electricity.
4. Evaluate the parameters that influence the performance of transmission line and to calculate performance parameters of various transmission lines.
5. Explain carona and its effects, underground cable and its construction, classification, limitations and specifications.
6. Evaluate different types of distribution systems.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

- For the Assignment component of the CIE, there are 25 marks and for the Internal Assessment Test component, there are 25 marks.
- The first test will be administered after 40-50% of the syllabus has been covered, and the second test will be administered after 85-90% of the syllabus has been covered
- Any two assignment methods mentioned in the 22OB2.4, if an assignment is project-based then only one assignment for the course shall be planned. The teacher should not conduct two assignments at the end of the semester if two assignments are planned.
- For the course, CIE marks will be based on a scaled-down sum of two tests and other methods of assessment.

Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester-End Examination:

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (**duration 03 hours).**

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
3. The students have to answer 5 full questions, selecting one full question from each module.
4. Marks scored shall be proportionally reduced to 50 marks

Suggested Learning Resources:

Text Books:

1. A Course in Electrical Power, Sony Gupta and Bhatnagar, Dhanpat Rai
2. Principles of Power System, V.K. Mehta, Rohit Mehta, S. Chand, 1st Edition 2013

Reference Books:

1. Power System Analysis and Design, J. Duncan Gloverat el, Cengage Learning, 4th Edition 2008
2. Electrical power Generation, Transmission and Distribution, S.N. Singh, PHI, 2nd Edition,2009
3. Electrical Power, S.L.Uppal, Khanna Publication
4. Electrical Power Systems, C. L. Wadhwa, New Age, 5th Edition, 2009
5. Electrical Power Systems, Ashfaq Hussain, CBS Publication
6. Electric Power Distribution, A.S. Pabla, McGraw-Hill, 6th Edition,2012

Web links and Video Lectures (e-Resources):

- www.nptel.ac.in

Activity Based Learning (Suggested Activities in Class)/ Practical Based learning

- Visit to Power Stations, Receiving Stations.
- Seminars

Microcontrollers			
Course Code	BEE403	CIE Marks	50
Teaching Hours/Week (L:T:P: S)	3:0:2:0	SEE Marks	50
Total Hours of Pedagogy	40 hours Theory + 8-10 Lab slots	Total Marks	100
Credits	04	Exam Hours	03
Examination nature (SEE)	Theory		

Course objectives:

At the end of the course the student will be able to:

1. To explain the internal organization and working of Computers, microcontrollers and embedded processors.
2. Compare and contrast the various members of the 8051family.
3. To explain the registers of the 8051 microcontroller, manipulation of data using registers and MOV instructions.
4. To explain in detail the execution of 8051 Assembly language instructions and data types
5. To explain loop, conditional and unconditional jump and call, handling and manipulation of I/O instructions.
6. To explain different addressing modes of 8051, arithmetic, logic instructions, and programs.
7. To explain develop 8051C programs for time delay, I/O operations, I/O bit manipulation, logic.
8. To explain writing assembly language programs for data transfer, arithmetic, Boolean and logical instructions.
9. To explain writing assembly language programs for code conversions.
10. To explain writing assembly language programs using subroutines for generation of delays, counters, configuration of SFRs for serial communication and timers.
11. To perform interfacing of stepper motor and DC motor for controlling the speed.
12. To explain generation of different waveforms using DAC interface.

Teaching-Learning Process (General Instructions)

These are sample Strategies; that teachers can use to accelerate the attainment of the various course outcomes.

1. Lecturer method (L) needs not to be only traditional lecture method, but alternative effective teaching methods could be adopted to attain the outcomes.
2. Use of Video/Animation to explain functioning of various concepts.
3. Encourage collaborative (Group Learning) Learning in the class.
4. Ask at least three HOT (Higher order Thinking) questions in the class, which promotes critical thinking.
5. Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop design thinking skills such as the ability to design, evaluate, generalize, and analyze information rather than simply recall it.
6. Introduce Topics in manifold representations.
7. Show the different ways to solve the same problem with different circuits/logic and encourage the students to come up with their own creative ways to solve them.
8. Discuss how every concept can be applied to the real world-and when that's possible, it helps improve the students' understanding.

MODULE-1

8051 Microcontroller Basics: Inside the Computer, Microcontrollers and Embedded Processors, Block Diagram of 8051, PSW and Flag Bits, 8051 Register Banks and Stack, Internal Memory Organization of 8051, IO Port Usage in 8051, Types of Special Function Registers and their uses in 8051, Pins of 8051. Memory Address Decoding, 8031/51 Interfacing With External ROM And RAM.8051 Addressing Modes.

MODULE-2

Assembly Programming and Instruction of 8051: Introduction to 8051 assembly programming, Assembling and running an 8051 program, Data types and Assembler directives Arithmetic, logic instructions and programs, Jump, loop and call instructions, IO port programming.

MODULE-3

8051 Programming in C: Data types and time delay in 8051C, IO programming in 8051C, Logic operations in 8051 C, Data conversion program in 8051 C, Accessing code ROM space in 8051C, Data serialization using 8051C.

8051 Timer Programming in Assembly and C: Programming 8051 timers, Counter programming, Programming timers 0 and 1 in 8051 C.

MODULE-4

8051 Serial Port Programming in Assembly and C: Basics of serial communication, 8051 connection to RS232, 8051 serial port programming in assembly, serial port programming in 8051 C.

8051 Interrupt Programming in Assembly and C: 8051 interrupts, Programming timer, external hardware, serial communication interrupt, Interrupt priority in 8051/52, Interrupt programming in C.

MODULE-5

Interfacing: LCD interfacing, Keyboard interfacing.

ADC, DAC and Sensor Interfacing: ADC 0808 interfacing to 8051, Serial ADC Max1112 ADC interfacing to 8051, DAC interfacing, Sensor interfacing and signal conditioning.

Motor Control: Relay, PWM, DC and Stepper Motor: Relays and opt isolators, stepper motor interfacing, DC motor interfacing and PWM.

8051 Interfacing with 8255: Programming the 8255, 8255 interfacing, C programming for 8255.

PRACTICAL COMPONENT OF IPCC

Sl.NO	Experiments
	(to be carried out using discrete components)
Note: For the experiments 1 to 7, 8051 assembly programming is to be used.	
1	Arithmetic instructions: Addition, subtraction, multiplication and division. Square using MATLAB/simulink.
2	Data transfer – Program for block data movement, sorting, exchanging, finding largest element in an array.
3	Up/Down BCD/ Binary Counters
4	Boolean and logical instructions (bit manipulation).
5	Code conversion programs – BCD to ASCII, ASCII to BCD, ASCII to decimal, Decimal to ASCII, Hexa.
6	Programs to generate delay, Programs using serial port and on-chip timer/counters.
Note: Single chip solution for interfacing 8051 is to be with C Programs for the following experiments.	
7	Simulate and test a PWM controlled DC motor using Simscape.
8	Stepper motor interface for direction and speed control.
9	Alphanumerical LCD panel interface.
10	Generate different waveforms: Sine, Square, Triangular, Ramp using DAC interface.

Course outcomes (Course Skill Set):

At the end of the course, the student will be able to:

1. Outline the 8051 architecture, registers, internal memory organization, addressing modes.
2. Discuss 8051 addressing modes, instruction set of 8051, accessing data and I/O port programming.
3. Develop 8051C programs for time delay, I/O operations, I/O bit manipulation, logic and arithmetic operations, data conversion and timer/counter programming.
4. Summarize the basics of serial communication and interrupts, also develop 8051 programs for serial data communication and interrupt programming.
5. Program 8051to work with external devices for ADC, DAC, Stepper motor control, DC motor control
6. Develop various 8051 based projects.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%.

The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

CIE for the theory component of the IPCC (maximum marks 50)

- IPCC means practical portion integrated with the theory of the course.
- CIE marks for the theory component are **25 marks** and that for the practical component is **25 marks**.
- 25 marks for the theory component are split into **15 marks** for two Internal Assessment Tests (Two Tests, each of 15 Marks with 01-hour duration, are to be conducted) and **10 marks** for other assessment methods mentioned in 22OB4.2. The first test at the end of 40-50% coverage of the syllabus and the second test after covering 85-90% of the syllabus.
- Scaled-down marks of the sum of two tests and other assessment methods will be CIE marks for the theory component of IPCC (that is for **25 marks)**.
- The student has to secure 40% of 25 marks to qualify in the CIE of the theory component of IPCC.

CIE for the practical component of the IPCC

- **15 marks** for the conduction of the experiment and preparation of laboratory record, and **10 marks** for the test to be conducted after the completion of all the laboratory sessions.
- On completion of every experiment/program in the laboratory, the students shall be evaluated including viva-voce and marks shall be awarded on the same day.
- The CIE marks awarded in the case of the Practical component shall be based on the continuous evaluation of the laboratory report. Each experiment report can be evaluated for 10 marks. Marks of all experiments' write-ups are added and scaled down to **15 marks**.
- The laboratory test **(duration 02/03 hours)** after completion of all the experiments shall be conducted for 50 marks and scaled down to **10 marks.**
- Scaled-down marks of write-up evaluations and tests added will be CIE marks for the laboratory component of IPCC for **25 marks**.
- The student has to secure 40% of 25 marks to qualify in the CIE of the practical component of the IPCC.

SEE for IPCC

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (**duration 03 hours**)

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
3. The students have to answer 5 full questions, selecting one full question from each module.
4. Marks scored by the student shall be proportionally scaled down to 50 Marks

The theory portion of the IPCC shall be for both CIE and SEE, whereas the practical portion will have a CIE component only. Questions mentioned in the SEE paper may include questions from the practical component.

Suggested Learning Resources:

Books

1. The 8051 Microcontroller and Embedded Systems Using Assembly and C, Muhammad Ali Mazadi, Pearson, 2nd Edition, 2008.
2. The 8051 Microcontroller, Kenneth Ayala, Cengage, 3rd Edition, 2005.
3. Microcontrollers: Architecture, Programming, Interfacing and System Design, Raj Kamal, Pearson, 1st Edition, 2012.

Web links and Video Lectures (e-Resources):

- NPTEL course on 8051 microcontrollers:**https://nptel.ac.in/courses/108105102**
- You tube videos on 8051 microccontrollers
- 8051 programming online course: Complete 8051 Microcontroller Programming Course | Udemy

Activity Based Learning (Suggested Activities in Class)/ Practical Based learning

- Mini projects using 8051 microcontroller
- Seminars
- Quizzes
- Assignments

Template for Practical Course and if AEC is a practical Course

Electric Motors Lab			
Course Code	BEEL404	CIE Marks	50
Teaching Hours/Week (L:T:P: S)	0:0:2	SEE Marks	50
Credits	01	Total Marks	100
		Exam Hours	03
Examination nature (SEE)	Practical		

Course objectives:

- To perform tests on DC Machines to determine their characteristics.
- To study the different control methods for DC Motors.
- To conduct test for pre-determination of the performance characteristics of DC Machines.
- To conduct load test on single-phase and three-phase Induction Motor.
- To conduct test on Induction Motor to determine performance characteristics.
- To conduct test on synchronous motor to draw performance curves.

Sl. NO	Experiments
1	Load test on DC shunt motor to draw speed–torque and horse power–efficiency characteristics.
2	Speed control of DC shunt motor by armature and field control.
3	Swin burne's Test on DC motor.
4	Regenerative test on DC shunt machines.
5	Load test on three phase induction motor.
6	No-load and Blocked rotor test on three phase induction motor to draw (i) equivalent circuit and (ii) circle diagram. Determination of performance parameters at different load conditions.
7	Load test on induction generator.
8	Load test on single phase induction motor to draw output versus torque, current, power and efficiency characteristics.
9	Conduct suitable tests to draw thee equivalent circuit of single phase induction motor and determine performance parameters.
10	Conduct an experiment to draw V and Inverted V curves of synchronous motor at no load and load conditions.
11	Analyze current and load torque of DC Shunt Motor using Simscape
12	Model 3-phase induction motor using MATLAB and Simulink

Course outcomes (Course Skill Set):

At the end of the course the student will be able to:

1. Perform tests on DC Machines to determine their characteristics.
2. Control the DC Motors using different methods.
3. Pre-determination the performance characteristics of DC Machines.
4. Conduct load test on single-phase and three-phase Induction Motor and draw performance characteristics.
5. Conduct test on Induction Motor to determine performance characteristics.
6. Conduct test on synchronous motor to draw performance curves.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together

Continuous Internal Evaluation (CIE):

CIE marks for the practical course are**50 Marks**.

The split-up of CIE marks for record/ journal and test are in the ratio **60:40**.

- Each experiment is to be evaluated for conduction with an observation sheet and record write-up. Rubrics for the evaluation of the journal/write-up for hardware/software experiments are designed by the faculty who is handling the laboratory session and are made known to students at the beginning of the practical session.
- Record should contain all the specified experiments in the syllabus and each experiment write-up will be evaluated for 10 marks.
- Total marks scored by the students are scaled down to **30 marks** (60% of maximum marks).
- Weightage to be given for neatness and submission of record/write-up on time.
- Department shall conduct a test of 100 marks after the completion of all the experiments listed in the syllabus.
- In a test, test write-up, conduction of experiment, acceptable result, and procedural knowledge will carry a weightage of 60% and the rest 40% for viva-voce.
- The suitable rubrics can be designed to evaluate each student's performance and learning ability.
- The marks scored shall be scaled down to **20 marks** (40% of the maximum marks).

The Sum of scaled-down marks scored in the report write-up/journal and marks of a test is the total CIE marks scored by the student.

Semester End Evaluation (SEE):

- SEE marks for the practical course are 50 Marks.
- SEE shall be conducted jointly by the two examiners of the same institute, examiners are appointed by the Head of the Institute.
- The examination schedule and names of examiners are informed to the university before the conduction of the examination. These practical examinations are to be conducted between the schedule mentioned in the academic calendar of the University.
- All laboratory experiments are to be included for practical examination.
- (Rubrics) Breakup of marks and the instructions printed on the cover page of the answer script to be strictly adhered to by the examiners. **OR** based on the course requirement evaluation rubrics shall be decided jointly by examiners.

- Students can pick one question (experiment) from the questions lot prepared by the examiners jointly.
- Evaluation of test write-up/ conduction procedure and result/viva will be conducted jointly by examiners.

General rubrics suggested for SEE are mentioned here, writeup-20%, Conduction procedure and result in -60%, Viva-voce 20% of maximum marks. SEE for practical shall be evaluated for 100 marks and scored marks shall be scaled down to 50 marks (however, based on course type, rubrics shall be decided by the examiners)

Change of experiment is allowed only once and 15% of Marks allotted to the procedure part are to be made zero.

The minimum duration of SEE is 02 hours

Suggested Learning Resources:

- www.nptel.ac.in

Electrical Power Generation and Economics		Semester	IV
Course Code	BEE405A	CIE Marks	50
Teaching Hours/Week (L: T:P: S)	3:0:0:0	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	03	Exam Hours	03
Examination nature (SEE)	Theory		

Course objectives:

- To understand the basics of hydro electric power plant, merits and demerits of hydroelectric power plants, site selection, arrangement and elements of hydro electric plant.
- To understand the working, site selection and arrangement of Steam, Diesel and Gas Power Plants.
- To understand the working, site selection and arrangement of Nuclear Power Plants.
- To understand importance of different equipments in substation, Interconnection of power stations and different types of grounding.
- To understand the economics of power generation.

Teaching-Learning Process (General Instructions)

These are sample Strategies, which teachers can use to accelerate the attainment of the various course outcomes.

1. Lecturer method (L) needs not to be only traditional lecture method, but alternative effective teaching methods could be adopted to attain the outcomes.
2. Use of Video/Animation to explain functioning of various concepts.
3. Encourage collaborative (Group Learning) Learning in the class.
4. Ask at least three HOT (Higher order Thinking) questions in the class, which promotes critical thinking.
5. Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop design thinking skills such as the ability to design, evaluate, generalize, and analyze information rather than simply recall it.
6. Introduce Topics in manifold representations.
7. Show the different ways to solve the same problem with different circuits/logic and encourage the students to come up with their own creative ways to solve them.
8. Discuss how every concept can be applied to the real world-and when that's possible, it helps improve the students' understanding.

Module-1

Hydroelectric Power Plants: Hydrology, run off and stream flow, hydrograph, flow duration curve, Mass curve, reservoir capacity, dam storage. Hydrological cycle, merits and demerits of hydroelectric power plants, Selection of site. General arrangement of hydel plant, elements of the plant, Classification of the plants based on water flow regulation, water head and type of load the plant has to supply. Water turbines – Pelton wheel, Francis, Kaplan and propeller turbines. Characteristic of water turbines Governing of turbines, selection of water turbines. Underground, small hydro and pumped storage plants. Choice of size and number of units, plant layout and auxiliaries.

Module-2

Steam Power Plants: Introduction, Efficiency of steam plants, Merits and demerits of plants, selection of site. Working of steam plant, Power plant equipment and layout, Steam turbines, Fuels and fuel handling, Fuel combustion and combustion equipment, Coal burners, Fluidized bed combustion, Combustion control, Ash handling, Dust collection, Draught systems, Feed water, Steam power plant controls, plant auxiliaries.

Diesel Power Plant: Introduction, Merits and demerits, selection o f site, elements of diesel power plant, applications.

Gas Turbine Power Plant: Introduction Merits and demerits, selection of site, Fuels for gas turbines, Elements of simple gas turbine power plant, Methods of improving thermal efficiency of a simple gas power plant, Closed cycle gas turbine power plants. Comparison of gas power plant with steam and diesel power plants.

Module-3

Nuclear Power Plants: Introduction, Economics of nuclear plants, Merits and demerits, selection of site, Nuclear reaction, Nuclear fission process, Nuclear chain reaction, Nuclear energy, Nuclear fuels,Nuclear plant and layout, Nuclear reactor and its control, Classification of reactors, power reactors in use, Effects of nuclear plants, Disposal of nuclear waste and effluent, shielding.

Module-4

Substations: Introduction to Substation equipment; Transformers, High Voltage Fuses, High Voltage Circuit Breakers and Protective Relaying, High Voltage Disconnect Switches, Lightning Arresters, High Voltage Insulators and Conductors, Voltage Regulators, Storage Batteries, Reactors, Capacitors, Measuring Instruments, and power line carrier communication equipment. Classification of substations – indoor and outdoor, Selection of site for substation, Bus-bar arrangement schemes and single line diagrams of substations.

Interconnection of power stations. Introduction to gas insulated substation, Advantages and economics of Gas insulated substation.

Grounding: Introduction, Difference between grounded and ungrounded system. System grounding – ungrounded, solid grounding, resistance grounding, reactance grounding, resonant grounding. Earthing transformer. Neutral grounding and neutral grounding transformer.

Module-5

Economics: Introduction, Effect of variable load on power system, classification of costs, Cost analysis. Interest and Depreciation, Methods of determination of depreciation, Economics of Power generation, different terms considered for power plants and their significance, load sharing. Choice of size and number of generating plants. Tariffs, objective, factors affecting the tariff, types. Types of consumers and their tariff. Power factor, disadvantages, causes, methods of improving power factor, Advantages of improved power factor, economics of power factor improvement and comparison of methods of improving the power factor. Choice of equipment.

Course outcome (Course Skill Set)

At the end of the course, the student will be able to :

1. Explain the basics of hydro electric power plant, merits and demerits of hydroelectric power plants, site selection, arrangement and elements of hydro electric plant.
2. Explain the working, site selection and arrangement of Steam, Diesel and Gas Power Plants.
3. Explain the working, site selection and arrangement of Nuclear Power Plants.
4. Explain the importance of different equipments in substation, Interconnection of power stations and different types of grounding.
5. Explain the economics of power generation.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

- For the Assignment component of the CIE, there are 25 marks and for the Internal Assessment Test component, there are 25 marks.
- The first test will be administered after 40-50% of the syllabus has been covered, and the second test will be administered after 85-90% of the syllabus has been covered
- Any two assignment methods mentioned in the 22OB2.4, if an assignment is project-based then only one assignment for the course shall be planned. The teacher should not conduct two assignments at the end of the semester if two assignments are planned.
- For the course, CIE marks will be based on a scaled-down sum of two tests and other methods of assessment.

Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester-End Examination:

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (**duration 03 hours).**

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
3. The students have to answer 5 full questions, selecting one full question from each module.
4. Marks scored shall be proportionally reduced to 50 marks

Suggested Learning Resources:

Text Books

1. Power Plant Engineering, P.K. Nag, Mc Graw Hill, 4th Edition, 2014
2. Generation of Electrical Energy, B.R.Gupta, S. Chand, 2015
3. Electrical power Generation, Transmission and Distribution, S.N. Singh, PHI, 2nd Edition, 2009

Reference Books

1. A Course in Power Systems, J.B. Gupta, Katson, 2008
2. Electrical Power Distribution Systems, V. Kamaraju, McGrawHill, 1st Edition, 2009
3. A Text Book on Power SystemEngineering, A. Chakrabarti, et al, Dhanpath Rai, 2nd Edition, 2010
4. Electrical Distribution Engineering, Anthony J. Pansini, CRC Press, 3rd Edition, 2006
5. Electrical Distribution Systems, Dale R PatrickEt al, CRC Press, 2nd Edition, 2009

Web links and Video Lectures (e-Resources):

- www.nptel.ac.in

Activity Based Learning (Suggested Activities in Class)/ Practical Based learning

- Visit to power station.
- Walk through videos

OPAMPS AND LIC		Semester	IV
Course Code	BEE405B	CIE Marks	50
Teaching Hours/Week (L: T:P: S)	3:0:0:0	SEE Marks	50
Total Hours of Pedagogy	40 hours	Total Marks	100
Credits	03	Exam Hours	03
Examination nature (SEE)	Theory		

Course objectives:

- To understand the basics of Linear ICs such as Op-amp, Regulator, Timer & PLL.
- To learn the designing of various circuits using linear ICs.
- To use these linear ICs for specific applications.
- To understand the concept and various types of converters.
- To use these ICs, in Hardware projects.

Teaching-Learning Process (General Instructions)
These are sample Strategies, which teachers can use to accelerate the attainment of the various course outcomes.

1. Lecturer method (L) needs not to be only traditional lecture method, but alternative effective teaching methods could be adopted to attain the outcomes.
2. Use of Video/Animation to explain functioning of various concepts.
3. Encourage collaborative (Group Learning) Learning in the class.
4. Ask at least three HOT (Higher order Thinking) questions in the class, which promotes critical thinking.
5. Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop design thinking skills such as the ability to design, evaluate, generalize, and analyze information rather than simply recall it.
6. Introduce Topics in manifold representations.
7. Show the different ways to solve the same problem with different circuits/logic and encourage the students to come up with their own creative ways to solve them.
8. Discuss how every concept can be applied to the real world-and when that's possible, it helps improve the students' understanding.

Module-1

Operational amplifiers: Introduction, Block diagram representation of a typical Op-amp, schematicsymbol, characteristics of an Op-amp, ideal op-amp, equivalent circuit, ideal voltage transfercurve,open loop configuration, differential amplifier, inverting & non –inverting amplifier, Op-amp withnegative feedback ; voltage series feedback amplifier-gain, input resistance, output resistance,voltage shunt feedback amplifier- gain, input resistance, output resistance. **General Linear Applications**: D.C. & A.C amplifiers, peaking amplifier, summing, scaling & averaging amplifier, inverting and non-inverting configuration, differential configuration, instrumentation amplifier

Module-2

Active Filters: First & Second order high pass & low pass Butterworth filters, higher order filters, Band pass filters, Band reject filters & all pass filters.
DC Voltage Regulators: voltage regulator basics, voltage follower regulator, adjustable output regulator, LM317 & LM337 Integrated circuits regulators.

Module-3

Signal generators: Working and derivation of frequency of oscillation for Phase shift oscillator, Wien bridge oscillator, square wave generator, sawtooth wave generator, triangular wave generator, rectangular wave generator.
Comparators & Converters: Basic comparator, zero crossing detector, inverting & non-invertingSchmitt trigger circuit, voltage to current converter with grounded load, current to voltageconverterand basics of voltage to frequency and frequency to voltage converters.

Module-4
Signal processing circuits: Precision half wave & full wave rectifiers limiting circuits, clamping circuits, peak detectors, sample & hold circuits. **A/D & D/A Converters**: Basics, R–2R D/A Converter, Integrated circuit 8-bit D/A, successive approximation ADC, linear ramp ADC, dual slope ADC, digital ramp ADC
Module-5
Phase Locked Loop (PLL): Basic PLL, components, performance factors, applications of PLL IC 565. Timer: Internal architecture of 555 timer, Mono stable, Astable-multivibrators and applications

Course outcome (Course Skill Set)

At the end of the course, the student will be able to :

1. Explain the basics of linear ICs.
2. Design circuits using linear ICs.
3. Demonstrate the application of Linear ICs.
4. Use ICs in the electronic projects

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

- For the Assignment component of the CIE, there are 25 marks and for the Internal Assessment Test component, there are 25 marks.
- The first test will be administered after 40-50% of the syllabus has been covered, and the second test will be administered after 85-90% of the syllabus has been covered
- Any two assignment methods mentioned in the 22OB2.4, if an assignment is project-based then only one assignment for the course shall be planned. The teacher should not conduct two assignments at the end of the semester if two assignments are planned.
- For the course, CIE marks will be based on a scaled-down sum of two tests and other methods of assessment.
- Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester-End Examination:

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (duration 03 hours).

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), should have a mix of topics under that module.
3. The students have to answer 5 full questions, selecting one full question from each module.
4. Marks scored shall be proportionally reduced to 50 marks

Suggested Learning Resources:

Books

1. Op-Amps and Linear Integrated Circuits, Ramakant A Gayakwad , Pearson, 4th Edition, 2015
2. Operational Amplifiers and Linear ICs, David A. Bell ,Oxford, 3rd Edition 2011
3. Linear Integrated Circuits , S. Salivahanan, et al, Wiley India , 2013
4. Op-Amps and Linear Integrated Circuits, Concept and Application, James M Fiore, Cengage, 2009

Web links and Video Lectures (e-Resources):

- NPTEL course on opamps : https://nptel.ac.in/courses/108108114
- You tube videos on opamps and in Linear Integrated Circuits.

Activity Based Learning (Suggested Activities in Class)/ Practical Based learning

- To develop mini projects based on opamp
- To develop mini projects based on timer and PLL IC
- Seminars
- Quizzes
- Assignments

Engineering Materials		Semester	IV
Course Code	BEE405C	CIE Marks	50
Teaching Hours/Week (L:T:P: S)	3:0:0:0	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	03	Exam Hours	03
Examination nature (SEE)	Theory		

Course objectives:

- To understand wave particle duality, tunnelling phenomenon, electron theory of metals.
- To understand the free electron theory of conduction in metals.
- To understand the polarization under static fields, behavior of dielectrics in alternating fields, Inorganic materials, organic materials,), resins and varnishes, liquid insulators.
- To understand the mechanism of conduction in semiconductors.
- To understand the magnetic materials, their classification and magneto materials.

Teaching-Learning Process (General Instructions)

These are sample Strategies, which teachers can use to accelerate the attainment of the various course outcomes.

1. Lecturer method (L) needs not to be only traditional lecture method, but alternative effective teaching methods could be adopted to attain the outcomes.
2. Use of Video/Animation to explain functioning of various concepts.
3. Encourage collaborative (Group Learning) Learning in the class.
4. Ask at least three HOT (Higher order Thinking) questions in the class, which promotes critical thinking.
5. Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop design thinking skills such as the ability to design, evaluate, generalize, and analyse information rather than simply recall it.
6. Introduce Topics in manifold representations.
7. Show the different ways to solve the same problem with different circuits/logic and encourage the students to come up with their own creative ways to solve them.
8. Discuss how every concept can be applied to the real world - and when that's possible, it helps improve the students' understanding.

Module-1

THEORY OF METALS

Elementary Quantum mechanical ideas: Wave Particle Duality, Wave function, schrodinger's equation, operator notation, expected value, Infinite Potential Well: A confined electron. Finite Potential Barrier: Tunnelling Phenomenon. Free electron theory of metals: Electron in a linear solid, Fermi energy, Degenerate states, Number of States, Density of States, Population Density. Fermi-Dirac Distribution Function. Thermionic Emission: Richardson's Equation, Schottky Effect. Contact Potential: Fermi level at Equilibrium.

Module-2

FREE ELECTRON THEORY OF CONDUCTION IN METAL

Crystalline structure: Simple cubic structure, Body centered cubic, Face centered cubic. Band Theory of Solids. Effective mass of Electron. Thermal Velocity of Electron at equilibrium. Electron mobility, conductivity and resistivity.

Module-3

DIELECTRICS and INSULATING MATERIALS

DIELECTRICS: Dielectric, polarization under static fields- electronic ionic and dipolar polarizations, behavior of dielectrics in alternating fields, Factors influencing dielectric strength and capacitor materials. Insulating materials, complex dielectric constant, dipolar relaxation and dielectric loss.

INSULATING MATERIALS: Inorganic materials (mica, glass, porcelain, asbestos), organic materials (paper, rubber, cotton silk fiber, wood, plastics and bakelite), resins and varnishes, liquid insulators(transformer oil) gaseous insulators (air, SF6 and nitrogen) and ageing of insulators.

Module-4

SEMICONDUCTORS

Mechanism of conduction in semiconductors, density of carriers in intrinsic semiconductors, the energy gap, types of semiconductors. Hall effect, compound semiconductors, basic ideas of amorphous and organic semiconductors.

Module-5

Magnetic materials

Magnetic materials: Classification of magnetic materials- origin of permanent magnetic dipoles, ferromagnetism, Magnetic Domains: Domain structure, Domain Wall motion, Hysteresis loop, Eddy current losses, Demagnetization, hard and soft magnetic materials, magneto materials used in electrical machines, instruments and relays.

Course outcome (Course Skill Set)

At the end of the course, the student will be able to :

1. Explain wave particle duality, tunnelling phenomenon, electron theory of metals.
2. Explain the free electron theory of conduction in metals.
3. Explain the polarization under static fields, behavior of dielectrics in alternating fields, Inorganic materials, organic materials,), resins and varnishes, liquid insulators.
4. Explain the mechanism of conduction in semiconductors.
5. Explain the magnetic materials, their classification and magneto materials.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

- For the Assignment component of the CIE, there are 25 marks and for the Internal Assessment Test component, there are 25 marks.
- The first test will be administered after 40-50% of the syllabus has been covered, and the second test will be administered after 85-90% of the syllabus has been covered
- Any two assignment methods mentioned in the 22OB2.4, if an assignment is project-based then only one assignment for the course shall be planned. The teacher should not conduct two assignments at the end of the semester if two assignments are planned.
- For the course, CIE marks will be based on a scaled-down sum of two tests and other methods of assessment.

Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester-End Examination:

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (**duration 03 hours).**

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
3. The students have to answer 5 full questions, selecting one full question from each module.
4. Marks scored shall be proportionally reduced to 50 marks

Suggested Learning Resources:

Books

1. Bhadra Prasad Pokharel and Nava Raj Karki,"Electrical Engineering Materials", Sigma offset Press, Kamaladi, Kathmandu, Nepal,2004.
2. R.C. Jaeger, "Introduction to Microelectronic Fabrication- Volume IV", Addison Wesley publishing Company,Inc., 1988.
3. Introduction to Electrical Engineering Materials 4th Edn. 2004 Edition by Indulkar C, S. Chand & Company Ltd-New Delhi.
4. Electrical and Electronic Engineering Materials by SK Bhattacharya, Khanna Publishers, New Delhi.

Web links and Video Lectures (e-Resources):

- www.nptel.ac.in

Activity Based Learning (Suggested Activities in Class)/ Practical Based learning

- Seminars
- Quizzes

Object Oriented Programming		Semester	IV
Course Code	BEE405D	CIE Marks	50
Teaching Hours/Week (L: T:P: S)	3:0:0:0	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	03	Exam Hours	03
Examination nature (SEE)	Theory		

Course objectives:

- To get a clear understanding of object-oriented concepts.
- To understand object oriented programming through C++

Teaching-Learning Process (General Instructions)

These are sample Strategies, which teachers can use to accelerate the attainment of the various course outcomes.

1. Lecturer method (L) needs not to be only traditional lecture method, but alternative effective teaching methods could be adopted to attain the outcomes.
2. Use of Video/Animation to explain functioning of various concepts.
3. Encourage collaborative (Group Learning) Learning in the class.
4. Ask at least three HOT (Higher order Thinking) questions in the class, which promotes critical thinking.
5. Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop design thinking skills such as the ability to design, evaluate, generalize, and analyze information rather than simply recall it.
6. Introduce Topics in manifold representations.
7. Show the different ways to solve the same problem with different circuits/logic and encourage the students to come up with their own creative ways to solve them.
8. Discuss how every concept can be applied to the real world-and when that's possible, it helps improve the students' understanding.

Module-1

Overview:

Why Object-Oriented Programming in C++ - Native Types and Statements –Functions and Pointers Implementing ADTs in the Base Language.

Module-2

BASIC CHARACTERISTICS OF OOP:

Data Hiding and Member Functions- Object Creation and Destruction- Polymorphism data abstraction: Iterators and Containers.

Module-3

ADVANCED PROGRAMMING:

Templates, Generic Programming, and STL-Inheritance-Exceptions-OOP Using C++.

Module-4

OVERVIEW OF JAVA:

Data types, variables and arrays, operators, control statements, classes, objects, methods – Inheritance

Module-5

EXCEPTION HANDLING:

Packages and Interfaces, Exception handling, Multithreaded programming, Strings, Input/Output

Course outcome (Course Skill Set)

At the end of the course, the student will be able to :

1. Discuss the basic Object Oriented concepts.
2. Develop applications using Object Oriented Programming Concepts.
3. Implement features of object oriented programming to solve real world problems.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

- For the Assignment component of the CIE, there are 25 marks and for the Internal Assessment Test component, there are 25 marks.
- The first test will be administered after 40-50% of the syllabus has been covered, and the second test will be administered after 85-90% of the syllabus has been covered
- Any two assignment methods mentioned in the 22OB2.4, if an assignment is project-based then only one assignment for the course shall be planned. The teacher should not conduct two assignments at the end of the semester if two assignments are planned.
- For the course, CIE marks will be based on a scaled-down sum of two tests and other methods of assessment.

Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester-End Examination:

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (**duration 03 hours).**

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
3. The students have to answer 5 full questions, selecting one full question from each module.
4. Marks scored shall be proportionally reduced to 50 marks

Suggested Learning Resources:

Text Books

1. Ira Pohl, "Object-Oriented Programming Using C++", Pearson Education Asia, 2003.
2. H.M.Deitel, P.J.Deitel, "Java : how to program", Fifth edition, Prentice Hall of India private limited, 2003.

Reference Books

1. Herbert Schildt, "The Java 2: Complete Reference", Fourth edition, TMH, 2002
2. Bjarne Stroustrup, "The C++ Programming Language", Pearson Education, 2004.
3. Stanley B. Lippman and Josee Lajoie , "C++ Primer", Pearson Education, 2003.
4. K.R.Venugopal, Rajkumar Buyya, T.Ravishankar, "Mastering C++", TMH, 2003.

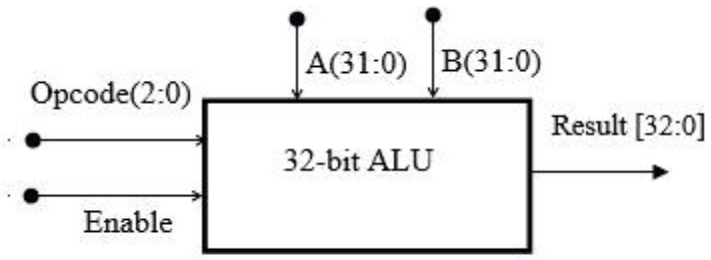
Web links and Video Lectures (e-Resources):

- www.nptel.ac.in

BASICS OF –VHDL LAB		Semester	IV
Course Code	**BEE456A**	CIE Marks	50
Teaching Hours/Week (L:T:P: S)	0:0:2:0	SEE Marks	50
Credits	01	Exam Hours	03
Examination nature (SEE)	Practical/Viva-Voce		

Course objectives:

1. Along with prescribed hours of teaching –learning process, provide opportunity to perform the experiments/programmes at their own time, at their own pace, at any place as per their convenience and repeat any number of times to understand the concept.
2. Provide unhindered access to perform whenever the students wish.
3. Vary different parameters to study the behaviour of the circuit without the risk of damaging equipment/device or injuring themselves.

Sl.NO	Experiments
	Note: Programming can be done using any compiler. Download the programs on a FPGA/CPLD board and performance testing may be done using 32 channel pattern generator and logic analyser, apart from verification by simulation with tools such as Altera/Modelsim or equivalent
1	Write Verilog program for the following combinational design along with test bench to verify the design: a) 2 to 4 decoder realization using NAND gates only (structural model) b) 8 to 3 encoder with priority encoder and without priority encoder (behavioral model) c) 8 to 1 Multiplexer using case statement and if statement d) 4 bit binary to gray code converter using 1 bit gray to binary converter 1 bit adder and subtractor.
2	Model in Verilog for a full adder and add functionality to perform logical operations of XOR, XNOR, AND and OR gates. Write test bench with appropriate input patterns to verify the modelled behavior.
3	Verilog 32 bit ALU shown in figure below and verify the functionality of ALU by selecting appropriate test patterns. The functionality of the ALU is shown in Table-1. a) Write test bench to verify the functionality of the ALU considering all possible input patterns b) The enable signal will set the output to required functions if enabled, if disabled all the outputs are set to tri-state. c) The acknowledge signal is set high after every operation is complete. 

<table>
<tr><td></td><td>ALU Top Level Diagram
Table -1 ALU functions:
<table>
<tr><th>Opcode (2:0)</th><th>ALU Operation</th><th colspan="2">Remarks</th></tr>
<tr><td>000</td><td>A + B</td><td>Addition of two numbers</td><td rowspan="2">Both A and B are in two's complement format</td></tr>
<tr><td>001</td><td>A – B</td><td>Subtraction of two numbers</td></tr>
<tr><td>010</td><td>A + 1</td><td>Increment Accumulator by 1</td><td rowspan="2">A is in two's complement format</td></tr>
<tr><td>011</td><td>A - 1</td><td>Decrement accumulator by 1</td></tr>
<tr><td>100</td><td>A</td><td>True</td><td rowspan="4">Inputs can be in any format</td></tr>
<tr><td>101</td><td>A Complement</td><td>Complement</td></tr>
<tr><td>110</td><td>A OR B</td><td>Logical OR</td></tr>
<tr><td>111</td><td>A AND B</td><td>Logical AND</td></tr>
</table></td></tr>
<tr><td>4</td><td>Write Verilog code for SR, D and JK and verify the flip flop</td></tr>
<tr><td>5</td><td>Write Verilog code for 4 bit BCD synchronous counter</td></tr>
<tr><td>6</td><td>Write Verilog code for counter with given input clock and check whether it works as clock divider performing division of clock by 2, 4, 8 and 16 . Verify the functionality of the code.</td></tr>
<tr><td></td><td>PART B
Note;
Interfacing and Debugging:
(ED) WinXp, PSpice, MultiSim, Proteus, CircuitLab, or any other equivalent tool can be used.</td></tr>
<tr><td></td><td>Demonstration Experiments (For CIE)</td></tr>
<tr><td>7</td><td>Write a Verilog code to design a clock divider circuit that generates ½, 1/3rd, 1/4th ,clock from given input clock . Port the design to FPGA and validate the functionality through CRO.</td></tr>
<tr><td>8</td><td>Interface a DC motor to FPGA and write Verilog code to change its speed and direction</td></tr>
<tr><td>9</td><td>Interface a stepper motor to FPGA and write Verilog code to control the stepper motor rotation which in turn may control a Robatic arm. External switches to be used for different controls like rotate the stepper motor:
a)+ N steps if the switch number 1 of a DIP switch is closed.
b)+N/2 steps if switch number 2 of a DIP switch is closed.
c)-N steps if switch number 3 of a DIP switch is closed etc.</td></tr>
<tr><td>10</td><td>Interface a DAC to FPGA and write Verilog code to generate a sine wave of frequency f KHz, ex f = 100 KHz, or 200 KHz etc, . Modify the code to down sample the frequency to f/2 KHz.
Display the original and down sampled signals by connecting them to CRO.</td></tr>
<tr><td>11</td><td>Write Verilog code using FSM to simulate elevator operation.</td></tr>
<tr><td>12</td><td>Write Verilog code to convert an analog input signal of a sensor to digital form and to display the same on a suitable display like simple set of LEDs , 7 segment display digits or LCD display</td></tr>
</table>

Course outcomes (Course Skill Set):
At the end of the course the student will be able to:

1. Write the VHDL/Verilog programs to simulate combinational circuits in data flow, behavioral, gate level abstractions.
2. Describe sequential circuits like flip-flops, counters, in behavioral descriptions and obtain simulated waveforms.
3. Use FPGA/CPLD kits for downloading Verilog codes and check output.
4. Synthesize combinational and sequential circuits on programmable ICs and test the hardware
5. Interface the hardware programmable chips and obtain the required output.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together

Continuous Internal Evaluation (CIE):

CIE marks for the practical course are**50 Marks**.

The split-up of CIE marks for record/ journal and test are in the ratio **60:40**.

- Each experiment is to be evaluated for conduction with an observation sheet and record write-up. Rubrics for the evaluation of the journal/write-up for hardware/software experiments are designed by the faculty who is handling the laboratory session and are made known to students at the beginning of the practical session.
- Record should contain all the specified experiments in the syllabus and each experiment write-up will be evaluated for 10 marks.
- Total marks scored by the students are scaled down to **30 marks** (60% of maximum marks).
- Weightage to be given for neatness and submission of record/write-up on time.
- Department shall conduct a test of 100 marks after the completion of all the experiments listed in the syllabus.
- In a test, test write-up, conduction of experiment, acceptable result, and procedural knowledge will carry a weightage of 60% and the rest 40% for viva-voce.
- The suitable rubrics can be designed to evaluate each student's performance and learning ability.
- The marks scored shall be scaled down to **20 marks** (40% of the maximum marks).

The Sum of scaled-down marks scored in the report write-up/journal and marks of a test is the total CIE marks scored by the student.

Semester End Evaluation (SEE):

- SEE marks for the practical course are 50 Marks.
- SEE shall be conducted jointly by the two examiners of the same institute, examiners are

appointed by the Head of the Institute.

- The examination schedule and names of examiners are informed to the university before the conduction of the examination. These practical examinations are to be conducted between the schedule mentioned in the academic calendar of the University.
- All laboratory experiments are to be included for practical examination.
- (Rubrics) Breakup of marks and the instructions printed on the cover page of the answer script to be strictly adhered to by the examiners. **OR** based on the course requirement evaluation rubrics shall be decided jointly by examiners.
- Students can pick one question (experiment) from the questions lot prepared by the examiners jointly.
- Evaluation of test write-up/ conduction procedure and result/viva will be conducted jointly by examiners.

General rubrics suggested for SEE are mentioned here, writeup-20%, Conduction procedure and result in -60%, Viva-voce 20% of maximum marks. SEE for practical shall be evaluated for 100 marks and scored marks shall be scaled down to 50 marks (however, based on course type, rubrics shall be decided by the examiners)

Change of experiment is allowed only once and 15% of Marks allotted to the procedure part are to be made zero.

The minimum duration of SEE is 02 hours

Suggested Learning Resources:

- HDL Programming fundamentals , VHDL and Verilog, N. Botros, Cengage Learning,

Scilab / MATLAB for Electrical and Electronic Measurements			
Course Code	**BEEL456B**	CIE Marks	50
Teaching Hours/Week (L:T:P: S)	0:0:2:0	SEE Marks	50
Credits	01	Exam Hours	02

Course objectives:

(1) Along with prescribed hours of teaching –learning process, provide opportunity to perform the experiments/programmes at their own time, at their own pace, at any place as per their convenience and repeat any number of times to understand the concept.

(2) Provide unhindered access to perform whenever the students wish.

(3) Vary different parameters to study the behaviour of the circuit without the risk of damaging equipment/ device or injuring themselves.

Sl. NO	Experiments
1	Design and Analysis of measurement of Resistance using Wheatstone and Kelvins double bridge.
2	Design and Analysis of measurement of Inductance using Schering and De-Sauty's Bridges.
3	Design and Analysis of measurement of Inductance using Maxwells and Anderson Bridges.
4	Design and Analysis of measurement of Frequency in Single and Three Phase Circuits.
5	Design and Analysis of measurement of Real Power, Reactive and Power Factor in Three Phase Circuits.
6	Design and Analysis of measurement of Energy in Three Phase Circuits.
7	Design and Analysis of measurement of Flux and Flux density.
8	Testing and Analysis of Current Transformer using Silsbees Deflection Method.
9	Testing and Analysis of Voltage Transformer using Silsbees Deflection Method.
10	Design and Analysis of True RMS Reading Volt Meters.
11	Design and Analysis of Integrating and Successive approximation type Digital Volt Meters.
12	Design and Analysis of Q Meter.

Course outcomes (Course Skill Set):

At the end of the course the student will be able to:

- Analyse in a systematic way, think better, and perform better.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each course. The student has to secure not less than 35% (18 Marks out of 50) in the semester-end examination (SEE).

Continuous Internal Evaluation (CIE):

CIE marks for the practical course is **50 Marks**.

The split-up of CIE marks for record/ journal and test are in the ratio **60:40**.

- Each experiment to be evaluated for conduction with observation sheet and record write-up. Rubrics for the evaluation of the journal/write-up for hardware/software experiments designed by the faculty who is handling the laboratory session and is made known to students at the beginning of the practical session.
- Record should contain all the specified experiments in the syllabus and each experiment write-up will be evaluated for 10 marks.
- Total marks scored by the students are scaled downed to 30 marks (60% of maximum marks).
- Weightage to be given for neatness and submission of record/write-up on time.

- Department shall conduct 02 tests for 100 marks, the first test shall be conducted after the 8th week of the semester and the second test shall be conducted after the 14th week of the semester.
- In each test, test write-up, conduction of experiment, acceptable result, and procedural knowledge will carry a weightage of 60% and the rest 40% for viva-voce.
- The suitable rubrics can be designed to evaluate each student's performance and learning ability. Rubrics suggested in Annexure-II of Regulation book
- The average of 02 tests is scaled down to **20 marks** (40% of the maximum marks).
- The Sum of scaled-down marks scored in the report write-up/journal and average marks of two tests is the totalCIE marks scored by the student.

Semester End Evaluation (SEE):

- SEE marks for the practical course is 50 Marks.
- SEE shall be conducted jointly by the two examiners of the same institute, examiners are appointed by theUniversity
- All laboratory experiments are to be included for practical examination.
- (Rubrics) Breakup of marks and the instructions printed on the cover page of the answer script to be strictly adhered to by the examiners. **OR** based on the course requirement evaluation rubrics shall be decided jointlyby examiners.
- Students can pick one question (experiment) from the questions lot prepared by the internal /external examiners jointly.
- Evaluation of test write-up/ conduction procedure and result/viva will be conducted jointly by examiners. General rubrics suggested for SEE are mentioned here, writeup-20%, Conduction procedure and result in -60%, Viva-voce 20% of maximum marks. SEE for practical shall be evaluated for 100 marks and scored marks shall be scaled down to 50 marks (however, based on course type, rubrics shall be decided by theexaminers)
- Change of experiment is allowed only once and 15% Marks allotted to the procedure part to be made zero.The duration of SEE is 03 hours
- Rubrics suggested in Annexure-II of Regulation book.

PCB Design Laboratory			
Course Code	**BEEL456C**	CIE Marks	50
Teaching Hours/Week (L:T:P: S)	0:0:2:0	SEE Marks	50
Credits	01	Exam Hours	02

Course objectives:

(1) Along with prescribed hours of teaching –learning process, provide opportunity to perform the experiments/programmes at their own time, at their own pace, at any place as per their convenience and repeat any number of times to understand the concept.

(2) Provide unhindered access to perform whenever the students wish.

(3) Vary different parameters to study the behaviour of the circuit without the risk of damaging equipment/device or injuring themselves.

Sl. NO	Experiments	% Portion Coverage
1	**Introduction** Need for PCB, Types of PCBs : Single and Multilayer, Technology: Plated Through Hole, Surface Mount, PCB Material, Electronic Component packaging, PCB Designing, Fabrication, Electronic Design Automation Tools: proteus, Orcad or any other tool.	30%
2	Introduction to proteus, Orcad or any other tool., Schematic entry / drawing, netlisting, layering, component foot print library selection & designing, design rules, component placing: Manual & automatic, track routing: automatic & manual, rules: track length, angle, joint & size, Autorouter setup. Design Rules.	30%
3	PCB Designing Practice : PCB Designing of Basic and Analog Electronic Circuits, PCB Designing of Power Supplies.	10%
4	Post Designing & PCB Fabrication Process: Printing the Design, Etching, Drilling, Interconnecting and Packaging electronic Circuits, Gerber Generation, Soldering and De-soldering, Component Mounting, PCB and Hardware Testing.	30%

Course outcomes (Course Skill Set):

At the end of the course the student will be able to:

- Analyse in an intelligent manner, think better, and perform better.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each course. The student has to secure not less than 35% (18 Marks out of 50) in the semester-end examination(SEE).

Continuous Internal Evaluation (CIE):

CIE marks for the practical course is **50 Marks**.

The split-up of CIE marks for record/ journal and test are in the ratio **60:40**.

- Each experiment to be evaluated for conduction with observation sheet and record write-up. Rubrics for the evaluation of the journal/write-up for hardware/software experiments designed by the faculty who is handling the laboratory session and is made known to students at the beginning of the practical session.
- Record should contain all the specified experiments in the syllabus and each experiment write-up will be evaluated for 10 marks.
- Total marks scored by the students are scaled downed to 30 marks (60% of maximum marks).
- Weightage to be given for neatness and submission of record/write-up on time.
- Department shall conduct 02 tests for 100 marks, the first test shall be conducted after the 8th week of the

semester and the second test shall be conducted after the 14th week of the semester.

- In each test, test write-up, conduction of experiment, acceptable result, and procedural knowledge will carry a weightage of 60% and the rest 40% for viva-voce.
- The suitable rubrics can be designed to evaluate each student's performance and learning ability. Rubrics suggested in Annexure-II of Regulation book
- The average of 02 tests is scaled down to **20 marks** (40% of the maximum marks).
- The Sum of scaled-down marks scored in the report write-up/journal and average marks of two tests is the totalCIE marks scored by the student.

- **Semester End Evaluation (SEE):**
- SEE marks for the practical course is 50 Marks.
- SEE shall be conducted jointly by the two examiners of the same institute, examiners are appointed by theUniversity
- All laboratory experiments are to be included for practical examination.
- (Rubrics) Breakup of marks and the instructions printed on the cover page of the answer script to be strictly adhered to by the examiners. **OR** based on the course requirement evaluation rubrics shall be decided jointlyby examiners.
- Students can pick one question (experiment) from the questions lot prepared by the internal /external examiners jointly.
- Evaluation of test write-up/ conduction procedure and result/viva will be conducted jointly by examiners. General rubrics suggested for SEE are mentioned here, writeup-20%, Conduction procedure and result in -60%, Viva-voce 20% of maximum marks. SEE for practical shall be evaluated for 100 marks and scored marks shall be scaled down to 50 marks (however, based on course type, rubrics shall be decided by theexaminers)
- Change of experiment is allowed only once and 15% Marks allotted to the procedure part to be made zero.The duration of SEE is 03 hours
- Rubrics suggested in Annexure-II of Regulation book.

ARDUINO AND RASPBERRY PI		Semester	IV
Course Code	BEEL456D	CIE Marks	50
Teaching Hours/Week (L:T:P: S)	0:0:2:0	SEE Marks	50
Credits	01	Exam Hours	100
Examination type (SEE)	Practical		

Course objectives:

- Course objectives: To impart necessary and practical knowledge of components of Internet of Things
- To develop skills required to build real-life IoT based projects

Sl.No	Experiments
1	i) To interface LED/Buzzer with Arduino/Raspberry Pi and write a program to 'turn ON' LED for 1 sec after every 2 seconds. ii) To interface Push button/Digital sensor (IR/LDR) with Arduino/Raspberry Pi and write a program to 'turn ON' LED when push button is pressed or at sensor detection.
2	i) To interface DHT11 sensor with Arduino/Raspberry Pi and write a program to print temperature and humidity readings. ii) To interface OLED with Arduino/Raspberry Pi and write a program to print temperature and humidity readings on it.
3	To interface motor using relay with Arduino/Raspberry Pi and write a program to 'turn ON' motor when push button is pressed
4	To interface Bluetooth with Arduino/Raspberry Pi and write a program to send sensor data to Smartphone using Bluetooth
5	To interface Bluetooth with Arduino/Raspberry Pi and write a program to turn LED ON/OFF when '1'/'0' is received from Smartphone using Bluetooth
6	Write a program on Arduino/Raspberry Pi to upload temperature and humidity data to thing speak cloud
7	Write a program on Arduino/Raspberry Pi to retrieve temperature and humidity data from thing speak cloud
8	Write a program on Arduino/Raspberry Pi to retrieve temperature and humidity data from thing speak cloud
9	Write a program on Arduino/Raspberry Pi to publish temperature data to MQTT broker
10	Write a program to create UDP server on Arduino/Raspberry Pi and respond with humidity data to UDP client when requested.
11	Write a program to create TCP server on Arduino/Raspberry Pi and respond with humidity data to TCP client when requested.
12	Write a program on Arduino/Raspberry Pi to subscribe to MQTT broker for temperature data and print it.

Course outcomes (Course Skill Set):

At the end of the course the student will be able to:

At the end of the course the student will be able to:

1. Explain the concepts of Internet of Things and its hardware and software components
2. Interface I/O devices, sensors & communication modules
3. Remotely monitor data and control devices
4. Develop real life IoT based projects.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together

Continuous Internal Evaluation (CIE):

CIE marks for the practical course are**50 Marks**.

The split-up of CIE marks for record/ journal and test are in the ratio **60:40**.

- Each experiment is to be evaluated for conduction with an observation sheet and record write-up. Rubrics for the evaluation of the journal/write-up for hardware/software experiments are designed by the faculty who is handling the laboratory session and are made known to students at the beginning of the practical session.
- Record should contain all the specified experiments in the syllabus and each experiment write-up will be evaluated for 10 marks.
- Total marks scored by the students are scaled down to **30 marks** (60% of maximum marks).
- Weightage to be given for neatness and submission of record/write-up on time.
- Department shall conduct a test of 100 marks after the completion of all the experiments listed in the syllabus.
- In a test, test write-up, conduction of experiment, acceptable result, and procedural knowledge will carry a weightage of 60% and the rest 40% for viva-voce.
- The suitable rubrics can be designed to evaluate each student's performance and learning ability.
- The marks scored shall be scaled down to **20 marks** (40% of the maximum marks).

The Sum of scaled-down marks scored in the report write-up/journal and marks of a test is the total CIE marks scored by the student.

Semester End Evaluation (SEE):

- SEE marks for the practical course are 50 Marks.
- SEE shall be conducted jointly by the two examiners of the same institute, examiners are appointed by the Head of the Institute.
- The examination schedule and names of examiners are informed to the university before the conduction of the examination. These practical examinations are to be conducted between the schedule mentioned in the academic calendar of the University.
- All laboratory experiments are to be included for practical examination.
- (Rubrics) Breakup of marks and the instructions printed on the cover page of the answer script to be strictly adhered to by the examiners. **OR** based on the course requirement evaluation rubrics shall be decided jointly by examiners.

- Students can pick one question (experiment) from the questions lot prepared by the examiners jointly.
- Evaluation of test write-up/ conduction procedure and result/viva will be conducted jointly by examiners.

General rubrics suggested for SEE are mentioned here, writeup-20%, Conduction procedure and result in -60%, Viva-voce 20% of maximum marks. SEE for practical shall be evaluated for 100 marks and scored marks shall be scaled down to 50 marks (however, based on course type, rubrics shall be decided by the examiners)

Change of experiment is allowed only once and 15% of Marks allotted to the procedure part are to be made zero.

The minimum duration of SEE is 02 hours

Suggested Learning Resources:

1. https://www.arduino.cc
2. https://www.raspberrypi.org/
3. Course in Internet of Things (IOT) Using Arduino - NIELIT Delhi Centre
4. Vijay Madisetti, Arshdeep Bahga, Internet of Things. "A Hands on Approach", University Press
5. Dr. SRN Reddy, Rachit Thukral and Manasi Mishra, "Introduction to Internet of Things: A practical Approach", ETI Labs
6. Pethuru Raj and Anupama C Raman, "The Internet of Things: Enabling Technologies, Platforms, and Use Cases", CRC Press
7. Jeeva Jose, "Internet of Things", Khanna Publishing House, Delhi
8. Adrian McEwen, "Designing the Internet of Things", Wiley
9. Raj Kamal, "Internet of Things: Architecture and Design", McGraw Hill

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V SEMESTER

Sl. No	Course and Course Code		Course Title	Teaching Department (TD) and Question Paper Setting Board (PSB)	Teaching Hours /Week				Examination				Credits
					Theory Lecture	Tutorial	Practical/ Drawing	Self -Study	Duration in hours	CIE Marks	SEE Marks	Total Marks	
					L	T	P	S					
1	HSMS	BEE501	Engineering Management and Entrepreneurship	Any branch /EEE	3	0	0		03	50	50	100	3
2	IPCC	BEE502	Signals & DSP	EEE	3	0	2		03	50	50	100	4
3	PCC	BEE503	Power Electronics	EEE	4	0	0		03	50	50	100	4
4	PCCL	BEEL504	Power Electronics Lab	EEE	0	0	2		03	50	50	100	1
5	PEC	BEE515x	Professional Elective Course	EEE	3	0	0		03	50	50	100	3
6	PROJ	BEE586	Mini Project	EEE	0	0	4		03	100		100	2
7	AEC	BRMK557	Research Methodology and IPR	Any Department	2	2	0		02	50	50	100	3
8	MC	BESK508	Environmental Studies	TD: Civil/Biotech/Chemistry PSB: As specified by the University	2	0	0		02	50	50	100	2
9	MC	BNSK559	National Service Scheme (NSS)	NSS coordinator	0	0	2			100		100	0
		BPEK559	Physical Education (PE) (Sports and Athletics)	Physical Education Director									
		BYOK559	Yoga	Yoga Teacher									
									Total	**550**	**350**	**900**	**22**

Professional Elective Course			
BEE515A	High Voltage Engineering	BEE515C	Electric Vehicle Fundamentals
BEE515B	Power Electronics for Renewable Energy Systems	BEE515D	Fundamentals of VLSI Design

PCC: Professional Core Course, **PCCL**: Professional Core Course laboratory, **UHV**: Universal Human Value Course, **MC**: Mandatory Course (Non-credit), **AEC**: Ability Enhancement Course, **SEC**: Skill Enhancement Course, **L:** Lecture, **T**: Tutorial, **P**: Practical **S= SDA**: Skill Development Activity, **CIE**: Continuous Internal Evaluation, **SEE**: Semester End Evaluation. **K :** The letter in the course code indicates common to al the stream of engineering. **PROJ**: Project /Mini Project. **PEC**: Professional Elective Course

Professional Core Course (IPCC): Refers to Professional Core Course Theory Integrated with practicals of the same course. Credit for IPCC can be 04 and its Teaching–Learning hours (L : T : P) can be considered as (3 : 0 : 2) or (2 : 2 : 2). The theory part of the IPCC shall be evaluated both by CIE and SEE. The practical part shall be evaluated by only CIE (no SEE). However, questions from the practical part of IPCC shall be included in the SEE question paper. For more details, the regulation governing the Degree of Bachelor of Engineering /Technology (B.E./B.Tech.) 2022-23

National Service Scheme /Physical Education/Yoga: All students have to register for any one of the courses namely National Service Scheme (NSS), Physical Education (PE)(Sports and Athletics), and Yoga(YOG) with the concerned coordinator of the course during the first week of III semesters. Activities shall be carried out between III semester to the VI semester (for 4 semesters). Successful completion of the registered course and requisite CIE score is mandatory for the award of the degree. The events shall be appropriately scheduled by the colleges and the same shall be reflected in the calendar prepared for the NSS, PE, and Yoga activities. These courses shall not be considered for vertical progression as well as for the calculation of SGPA and CGPA, but completion of the course is mandatory for the award of degree.

Mini-project work: Mini Project is a laboratory-oriented/hands on course that will provide a platform to students to enhance their practical knowledge and skills by the development of small systems/applications etc. Based on the ability/abilities of the student/s and recommendations of the mentor, a single discipline or a multidisciplinary Mini- project can be assigned to an individual student or to a group having not more than 4 students.

CIE procedure for Mini-project:

(i) Single discipline: The CIE marks shall be awarded by a committee consisting of the Head of the concerned Department and two faculty members of the Department, one of them being the Guide. The CIE marks awarded for the Mini-project work shall be based on the evaluation of the project report, project presentation skill, and question and answer session in the ratio of 50:25:25. The marks awarded for the project report shall be the same for all the batches mates.

(ii) Interdisciplinary: Continuous Internal Evaluation shall be group-wise at the college level with the participation of all the guides of the project.

The CIE marks awarded for the Mini-project, shall be based on the evaluation of the project report, project presentation skill, and question and answer session in the ratio 50:25:25. The marks awarded for the project report shall be the same for all the batch mates.

No SEE component for Mini-Project.

Professional Elective Courses (PEC): A professional elective (PEC) course is intended to enhance the depth and breadth of educational experience in the Engineering and Technology curriculum. Multidisciplinary courses that are added supplement the latest trend and advanced technology in the selected stream of engineering. Each group will provide an option to select one course. The minimum number of students' strengths for offering a professional elective is 10. However, this conditional shall not be applicable to cases where the admission to the program is less than 10.

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VI SEMESTER

Sl. No	Course and Course Code		Course Title	Teaching Department (TD) and Question Paper Setting Board (PSB)	Teaching Hours /Week				Examination				Credits
					Theory Lecture	Tutorial	Practical/ Drawing	Self -Study	Duration in hours	CIE Marks	SEE Marks	Total Marks	
					L	T	P	S					
1	IPCC	BEE601	Power system Analysis - I	EEE	3	0	2		03	50	50	100	4
2	PCC	BEE602	Control Systems	EEE	3	2	0		03	50	50	100	4
3	PEC	BEE613x	Professional Elective Course	EEE	3	0	0		03	50	50	100	3
4	OEC	BEE654x	Open Elective Course	EEE	3	0	0		03	50	50	100	3
5	PROJ	BEE685	Project Phase I	EEE	0	0	4		03	100	--	100	2
6	PCCL	BEEL606	Control System Lab	EEE	0	0	2		03	50	50	100	1
7	AEC/SDC	BEE657x	Ability Enhancement Course/Skill Development Course - V	EEE	If the course is Theory				01	50	50	100	1
					1	0	0						
					If course is practical				02				
					0	0	2						
8	MC	BNSK658	National Service Scheme (NSS)	NSS coordinator	0	0	2			100	---	100	0
		BPEK658	Physical Education (PE) (Sports and Athletics)	Physical Education Director									
		BYOK658	Yoga	Yoga Teacher									
9	MC	IKS	Indian Knowledge System		1	0	0			100	0	100	0
									Total	**500**	**300**	**800**	**18**

Professional Elective Course

BEE613A	Medium Voltage Substation Design	BEE613C	FACTS and HVDC Transmission
BEE613B	Embedded SystemDesign	BEE613D	Electric Motor and Drive Systems for Electric Vehicles

Open Elective Course			
BEE654A	Utilization of Electrical Power	BEE654C	Industrial Servo Control Systems
BEE654B	Technologies of Renewable Energy Sources	BEE654D	Semiconductor Devices
Ability Enhancement Course / Skill Enhancement Course-V			
BEE657A	Energy Management in Electric Vehicles	BEEL657C	Energy Audit Project
BEEL657B	Simulation of Control of Power Electronics Circuits	BEEL657D	Project on Renewable Energy Sources

PCC: Professional Core Course, **PCCL**: Professional Core Course laboratory, **UHV**: Universal Human Value Course, **MC**: Mandatory Course (Non-credit), **AEC**: Ability Enhancement Course, **SEC**: Skill Enhancement Course, **L:** Lecture, **T**: Tutorial, **P**: Practical **S= SDA**: Skill Development Activity, **CIE**: Continuous Internal Evaluation, **SEE**: Semester End Evaluation. **K :** The letter in the course code indicates common to all the stream of engineering. **PROJ**: Project /Mini Project. **PEC**: Professional Elective Course. **PROJ**: Project Phase -I, **OEC**: Open Elective Course

Professional Core Course (IPCC): Refers to Professional Core Course Theory Integrated with practicals of the same course. Credit for IPCC can be 04 and its Teaching–Learning hours (L : T : P) can be considered as (3 : 0 : 2) or (2 : 2 : 2). The theory part of the IPCC shall be evaluated both by CIE and SEE. The practical part shall be evaluated by only CIE (no SEE). However, questions from the practical part of IPCC shall be included in the SEE question paper. For more details, the regulation governing the Degree of Bachelor of Engineering /Technology (B.E./B.Tech.) 2022-23

National Service Scheme /Physical Education/Yoga: All students have to register for any one of the courses namely National Service Scheme (NSS), Physical Education (PE)(Sports and Athletics), and Yoga(YOG) with the concerned coordinator of the course during the first week of III semesters. Activities shall be carried out between III semester to the VI semester (for 4 semesters). Successful completion of the registered course and requisite CIE score is mandatory for the award of the degree. The events shall be appropriately scheduled by the colleges and the same shall be reflected in the calendar prepared for the NSS, PE, and Yoga activities. These courses shall not be considered for vertical progression as well as for the calculation of SGPA and CGPA, but completion of the course is mandatory for the award of degree.

Professional Elective Courses (PEC): A professional elective (PEC) course is intended to enhance the depth and breadth of educational experience in the Engineering and Technology curriculum. Multidisciplinary courses that are added supplement the latest trend and advanced technology in the selected stream of engineering. Each group will provide an option to select one course. The minimum number of students' strengths for offering professional electives is 10. However, this conditional shall not be applicable to cases where the admission to the program is less than 10. As there are 5 verticals with four courses in each vertical, **Mentors are required to guide students in deciding PEC as per verticals.**

Open Elective Courses:

Students belonging to a particular stream of Engineering and Technology are not entitled to the open electives offered by their parent Department. However, they can opt for an elective offered by other Departments, provided they satisfy the prerequisite condition if any. Registration to open electives shall be documented under the guidance of the Program Coordinator/ Advisor/Mentor. The minimum numbers of students' strength for offering Open Elective Course is 10. However, this condition shall not be applicable to class where the admission to the program is less than 10.

Project Phase-I : Students have to discuss with the mentor /guide and with their help he/she has to complete the literature survey and prepare the report and finally define the problem statement for the project work.

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SCHEME -A-VII SEMESTER (Swappable VII and VIII SEMESTER)

Sl. No	Course and Course Code		Course Title	Teaching Department (TD) and Question Paper Setting Board (PSB)	Teaching Hours /Week				Examination				Credits
					Theory Lecture	Tutorial	Practical/ Drawing	Self -Study	Duration in hours	CIE Marks	SEE Marks	Total Marks	
					L	T	P	S					
1	IPCC	BEE701	Switchgear and Protection	EEE	3	0	2		03	50	50	100	4
2	PCC	BEE702	Industrial Drives and Applications	EEE	4	0	0		03	50	50	100	4
3	IPCC	BEE703	Power system analysis- II	EEE	3	0	2		03	50	50	100	4
4	PEC	BEE714x	Professional Elective Course	EEE	3	0	0		03	50	50	100	3
5	OEC	BEE755x	Open Elective Course	EEE	3	0	0		03	50	50	100	3
6	PROJ	BEE786	Major Project Phase-II	EEE	0	0	12		03	100	100	200	6
										350	**350**	**700**	**24**

Professional Elective Course

BEE714A	Power System Operation and Control	BEE714C	Programmable Logic Controllers
BEE714B	AI Techniques for Electric and Hybrid Electric Vehicles	BEE714D	Big Data Analytics in Power Systems

Open Elective Course

BEE755A	Electric Vehicle Technologies	BEE755C	PLC and SCADA
BEE755B	Energy Conservation and Audit	BEE755D	Optimisation Techniques

PCC: Professional Core Course, **PCCL**: Professional Core Course laboratory, **PEC**: Professional Elective Course, **OEC**: Open Elective Course PR: Project Work, **L:** Lecture, **T**: Tutorial, **P**: Practical **S= SDA**: Skill Development Activity, **CIE**: Continuous Internal Evaluation, **SEE**: Semester End Evaluation. **TD-** Teaching Department, **PSB**: Paper Setting department, **OEC**: Open Elective Course, **PEC**: Professional Elective Course. **PROJ**: Project work

Note: VII and VIII semesters of IV years of the program

(1) Institutions can swap the VII and VIII Semester Schemes of Teaching and Examinations to accommodate research internships/ industry internships after the VI semester**.**

(2) Credits earned for the courses of VII and VIII Semester Scheme of Teaching and Examinations shall be counted against the corresponding semesters whether the VII or VIII semesters is completed during the beginning of the IV year or the later part of IV years of the program.

Professional Elective Courses (PEC): A professional elective (PEC) course is intended to enhance the depth and breadth of educational experience in the Engineering and Technology curriculum. Multidisciplinary courses that are added supplement the latest trend and advanced technology in the selected stream of engineering. Each group will provide an option to select one course. The minimum number of students' strengths for offering professional electives is 10. However, this conditional shall not be applicable to cases where the admission to the program is less than 10.

Open Elective Courses:

Students belonging to a particular stream of Engineering and Technology are not entitled to the open electives offered by their parent Department. However, they can opt for an elective offered by other Departments, provided they satisfy the prerequisite condition if any. Registration to open electives shall be documented under the guidance of the Program Coordinator/ Advisor/Mentor. The minimum numbers of students' strength for offering Open Elective Course is 10. However, this condition shall not be applicable to class where the admission to the program is less than 10.

PROJECT WORK (21XXP75): The objective of the Project work is

(i) To encourage independent learning and the innovative attitude of the students.

(ii) To develop interactive attitude, communication skills, organization, time management, and presentation skills.

(iii) To impart flexibility and adaptability.

(iv) To inspire team working.

(v) To expand intellectual capacity, credibility, judgment and intuition.

(vi) To adhere to punctuality, setting and meeting deadlines.

(vii) To install responsibilities to oneself and others.

(viii) To train students to present the topic of project work in a seminar without any fear, face the audience confidently, enhance communication skills, involve in group discussion to present and exchange ideas.

CIE procedure for Project Work:

(1) Single discipline: The CIE marks shall be awarded by a committee consisting of the Head of the concerned Department and two senior faculty members of the Department, one of whom shall be the Guide.

The CIE marks awarded for the project work, shall be based on the evaluation of the project work Report, project presentation skill, and question and answer session in the ratio 50:25:25. The marks awarded for the project report shall be the same for all the batch mates.

(2) Interdisciplinary: Continuous Internal Evaluation shall be group-wise at the college level with the participation of all guides of the college. Participation of external guide/s, if any, is desirable. The CIE marks awarded for the project work, shall be based on the evaluation of project work Report, project presentation skill, and question and answer session in the ratio 50:25:25. The marks awarded for the project report shall be the same for all the batch mates.

SEE procedure for Project Work: SEE for project work will be conducted by the two examiners appointed by the University. The SEE marks awarded for the project work shall be based on the evaluation of project work Report, project presentation skill, and question and answer session in the ratio 50:25:25.

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SCHEME -AVIIISEMESTER (Swappable VII and VIII SEMESTER)

Sl. No	Course and Course Code		Course Title	Teaching Department (TD) and Question Paper Setting Board (PSB)	Teaching Hours /Week				Examination				Credits
					Theory Lecture	Tutorial	Practical/ Drawing	Self -Study	Duration in hours	CIE Marks	SEE Marks	Total Marks	
					L	T	P	S					
1	PEC	BEE801x	**Professional Elective (Online Courses)**	EEE	3	0	0		03	50	50	100	3
2	OEC	BEE802x	**Open Elective (Online Courses)**	EEE	0	2	0		01	50	50	100	3
3	INT	BEE803	**Internship (Industry/Research) (14 - 20 weeks)**		0	0	12		03	100	100	200	10
										200	**200**	**400**	**16**

Professional Elective Course (Online courses)			
BEE801A	NPTEL /MOOCS	BEE801D	NPTEL /MOOCS
BEE801B	NPTEL /MOOCS	BEE801E	NPTEL /MOOCS
BEE801C	NPTEL /MOOCS		

Open Elective Courses (Online Courses)			
BEE802A	Industry suggested course/ MOOCS	BEE802C	NPTEL /MOOCS
BEE802B	Industry suggested course / MOOCS	BEE802D	NPTEL MOOCS

L: Lecture, **T**: Tutorial, **P**: Practical **S= SDA**: Skill Development Activity, **CIE**: Continuous Internal Evaluation, **SEE**: Semester End Evaluation. **TD-** Teaching Department, **PSB**: Paper Setting department, **OEC**: Open Elective Course, **PEC**: Professional Elective Course. **PROJ**: Project work, **INT**: Industry Internship / Research Internship / Rural Internship

Note: VII and VIII semesters of IV years of the program

Swapping Facility

- Institutions can swap VII and VIII Semester Scheme of Teaching and Examinations to accommodate **research internships/ industry internships/Rural Internship** after the VI semester**.**
- Credits earned for the courses of VII and VIII Semester Scheme of Teaching and Examinations shall be counted against the corresponding semesters whether VII or VIII semester is completed during the beginning of IV year or later part of IV year of the program.

Elucidation:

At the beginning of IV years of the program i.e., after VI semester, VII semester class work and VIII semester **Research Internship /Industrial Internship / Rural Internship** shall be permitted to be operated simultaneously by the University so that students have ample opportunity for an internship. In other words, a good percentage of the class shall attend VII semester classwork and a similar percentage of others shall attend to Research Internship or Industrial Internship or Rural Internship.

Research/Industrial /Rural Internship shall be carried out at an Industry, NGO, MSME, Innovation center, Incubation center, Start-up, center of Excellence (CoE), Study Centre established in the parent institute and /or at reputed research organizations/institutes.

The mandatory Research internship /Industry internship / Rural Internship is for 14 to 20 weeks. The internship shall be considered as a head of passing and shall be considered for the award of a degree. Those, who do not take up/complete the internship shall be declared to fail and shall have to complete it during the subsequent University examination after satisfying the internship requirements.

Research internship: A research internship is intended to offer the flavor of current research going on in the research field. It helps students get familiarized with the field and imparts the skill required for carrying out research.

Industry internship: Is an extended period of work experience undertaken by students to supplement their degree for professional development. It also helps them learn to overcome unexpected obstacles and successfully navigate organizations, perspectives, and cultures. Dealing with contingencies helps students recognize, appreciate, and adapt to organizational realities by tempering their knowledge with practical constraints.

Rural Internship: Rural development internship is an initiative of Unnat Bharat Abhiyan Cell, RGIT in association with AICTE to involve students of all departments studying in different academic years for exploring various opportunities in techno-social fields, to connect and work with Rural India for their upliftment.

The faculty coordinator or mentor has to monitor the student's internship progress and interact with them to guide for the successful completion of the internship.

The students are permitted to carry out the internship anywhere in India or abroad. University shall not bear any expenses incurred in respect of the internship.

With the consent of the internal guide and Principal of the Institution, students shall be allowed to carry out the internship at their hometown (**within or outside the state or abroad**), provided favorable facilities are available for the internship and the student remains regularly in contact with the internal guide. **University shall not bear any cost involved in carrying out the internship by students.** However, students can receive any financial assistance extended by the organization.

Professional Elective /Open Elective Course: These are ONLINE courses suggested by the respective Board of Studies. Details of these courses shall be made available for students on the VTU web portal.

VISVESVARAYA TECHNOLOGICAL UNIVERSITY, BELAGAVI

B.E. in the title of the program

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(Effective from the academic year 2023-24)

Scheme B-VI SEMESTER for the candidates who seek a two-semester internship with project work /Start-up

Sl. No	Course and Course Code		Course Title	Teaching Department (TD) and Question Paper Setting Board (PSB)	Teaching Hours /Week				Examination				Credits
					Theory Lecture	Tutorial	Practical/ Drawing	SDA	Duration in hours	CIE Marks	SEE Marks	Total Marks	
					L	T	P	S					
1	IPCC	BXX601	Power system Analysis - I		3	0	2		03	50	50	100	4
2	PCC	BXX602	Control Systems		4	0	0		03	50	50	100	4
3	PEC	BXX613x	Professional Elective Course		3	0	0		03	50	50	100	3
4	OEC	BXX654x	Open Elective Course		3	0	0		03	50	50	100	3
5	PCCL	BXXL606	Control System Lab		0	0	2		03	50	50	100	1
6	AEC/SDC	BXX657x	Ability Enhancement Course/Skill Development Course V		If the course is offered as a Theory: 1	0	0		01	50	50	100	1
					If course is offered as a practical: 0	0	2						
7	MC	BNSK658	National Service Scheme (NSS)	NSS coordinator	0	0	2			100	---	100	0
		BPEK658	Physical Education (PE) (Sports and Athletics)	Physical Education Director									
		BYOK658	Yoga	Yoga Teacher									
8	IKS	BIKS609	Indian Knowledge System		1	0	0		01	100	0	100	0
									Total	**500**	**300**	**800**	**16**

Professional Elective Course			
BEE613A	Medium Voltage Substation Design	BEE613C	FACTS and HVDC Transmission
BEE613B	Embedded SystemDesign	BEE613D	Electric Motor and Drive Systems for Electric Vehicles
Open Elective Course			
BEE654A	Utilization of Electrical Power	BEE654C	Industrial Servo Control Systems
BEE654B	Technologies of Renewable Energy Sources	BEE654D	Semiconductor Devices

Ability Enhancement Course / Skill Enhancement Course-V			
BEE657A	Energy Management in Electric Vehicles	BEEL657C	Project on Energy Audit
BEEL657B	Simulation of Control of Power Electronics Circuits	BEEL657D	Project on Renewable Energy Sources

VISVESVARAYA TECHNOLOGICAL UNIVERSITY, BELAGAVI

B.E. in the title of the program

Scheme of Teaching and Examinations2022

Outcome Based Education (OBE) and Choice Based Credit System (CBCS)

(Effective from the academic year 2023-24)

Scheme B VII and VIII semesters for the candidates who seek an internship with project work

Sl. No	Course and Course Code		Course Title	Teaching Department (TD) and Question Paper Setting Board (PSB)	Teaching Hours /Week				Examination				Credits
					Theory Lecture	Tutorial	Practical/ Drawing	SDA	Duration in hours	CIE Marks	SEE Marks	Total Marks	
					L	T	P	S					
1	IPCC	BXX701	To be completed in 5th/6th semester		3	0	2		03	50	50	100	4
2	IPCC	BXX702	To be completed in 5th /6th semester		3	0	2		03	50	50	100	4
3	PCC	BXX703	To be completed in the 6th semester		4	0	0		03	50	50	100	3
4	PEC	BXX714x	Professional Elective Course (MOOC Courses)		3	0	0		03	50	50	100	3
5	OEC	BXX755x	Open Elective Courses (MOOC courses)		3	0	0		01	50	50	100	3
1	PEC	Bxx801x	Professional Elective (MOOC Courses)		3	0	0		03	50	50	100	3
2	OEC	Bxx802x	Open Elective (MOOC Courses)		3	0	0		01	50	50	100	3
3	PROJ	BXX883	Project - outcome of training		0	0	12		03	100	100	200	9
4	INT	Bxx804	Internship (Industry/Research) (02 semesters)		0	0	12		03	100	100	200	10
										200	**200**	**400**	**42**

V Semester

Engineering Management & Entrepreneurship			Semester	V
Course and Course Code	HSMS	IBEE501	CIE Marks	50
Teaching Hours/Week (L:T:P: S)	3:0:0:0		SEE Marks	50
Total Hours of Pedagogy	40 hours		Total Marks	100
Credits	3		Exam Hours	3
Examination nature (SEE)	Theory			

Course objectives:

After completion of the course, the students will be able to

- Understand basic skills of Management
- Understand the need for Entrepreneurs and their skills
- Identify the Management functions and Social responsibilities.
- Understand the identification of Business, drafting the Business plan and sources of funding.

Teaching-Learning Process (General Instructions)

These are sample Strategies; that teachers can use to accelerate the attainment of the various course outcomes.

- Lecture method (L) does not mean only the traditional lecture method, but a different type of teaching method may be adopted to develop the outcomes.
- Show Video/animation films to explain the functioning of various techniques.
- Encourage collaborative (Group) Learning in the class
- Ask at least three HOTS (Higher-order Thinking) questions in the class, which promotes critical thinking
- Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop thinking skills such as the ability to evaluate, generalize, and analyze information rather than simply recall it.
- Topics will be introduced in multiple representations.
- Show the different ways to solve the same problem and encourage the students to come up with their own creative ways to solve them.
- Discuss how every concept can be applied to the real world - and when that's possible, it helps improve the students' understanding.

MODULE – 1

Management: Nature and Functions of Management – Importance, Definition, Management Functions, Levels of Management, Roles of Manager, Managerial Skills, Management & Administration, Management as a Science, Art & Profession (Selected topics of Chapter 1, Text 1).

Planning: Planning-Nature, Importance, Types, Steps and Limitations of Planning; Decision Making – Meaning, Types and Steps in Decision Making(Text 1).

Teaching-Learning Process	Chalk and talk method, YouTube Videos, Power Point Presentation.
RBT Levels	L2, L3

MODULE – 2

Organizing and Staffing: Organization-Meaning, Characteristics, Process of Organizing, Principles of Organizing, Span of Management (meaning and importance only), Departmentalization-Process Departmentalization, Purpose Departmentalization ,Committees– Meaning, Types of Committees.

Staffing-Need and Importance, Recruitment and Selection Process.

Directing and Controlling: Meaning and Requirements of Effective Direction, Giving Orders; Motivation-Nature of Motivation, Motivation Theories (Maslow's Need-Hierarchy Theory and Herzberg's Two Factor Theory); Communication – Meaning, Importance and Purposes of Communication (Text 1).

Teaching-Learning Process	Chalk and talk method, YouTube Videos, Power Point Presentation.
RBT Levels	L2, L3

MODULE – 3

Leadership-Meaning, Characteristics, Behavioural Approach of Leadership; Coordination-Meaning, Types, Techniques of Coordination; Controlling – Meaning, Need for Control System, Benefits of Control, Essentials of Effective Control System, Steps in Control Process (Text 1).

Social Responsibilities of Business: Meaning of Social Responsibility, Social Responsibilities of Business towards Different Groups, Social Audit, Business Ethics and Corporate Governance (Text 1).

Teaching-Learning Process	Chalk and talk method, YouTube Videos, Power Point Presentation.
RBT Levels	L1, L2, L3

MODULE – 4

Entrepreneurship: Introduction, Evolution of the concept of Entrepreneurship, Entrepreneurship today, Types of Entrepreneurs, Entrepreneurship, Entrepreneurial competencies, Capacity Building for Entrepreneurs.

Identification of Business Opportunities: Introduction, Mobility of Entrepreneurs, Business opportunities in India, Models for opportunity Evaluation.

Teaching-Learning Process	Chalk and talk method, YouTube Videos, Power Point Presentation.
RBT Levels	L1, L2, L3

MODULE – 5

Business plans: Introduction, purpose of a Business plan, contents of a Business plan, presenting a Business plan, why do some Business plan fail? Procedure for setting up an Enterprise.

Institutions supporting Business opportunities: Central level institutions- National Board for micro, small & medium Enterprises(NBMSME),MSME-DO, National Small Industries Corporation. State level institutions- state Directorate Industries and commerce, District Industries Centres, state financial Corporations, State Industrial Development Corporation(SIDC), State Industrial Area Development Board (SIADB). Other Institutions - NABARD, Technical consultancy organisation (TCO), Small Industries Development Bank of India(SIDBI), Export Promotion Councils, Non governmental Organisations.

Teaching-Learning Process	Chalk and talk method, YouTube Videos, Power Point Presentation.
RBT Levels	L1, L2, L3

Course outcomes (Course Skill Set):

At the end of the course, the student will be able to:

1) Understand the fundamental concepts of Management and its functions.
2) Understand the different functions to be performed by managers/Entrepreneur.
3) Understand the social responsibilities of a Business.
4) Understand the Concepts of Entrepreneurship and to identify Business opportunities.
5) Understand the components in developing a business plan and awareness about various sources of funding and Institutions supporting Entrepreneur.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/

course if the student secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

- For the Assignment component of the CIE, there are 25 marks and for the Internal Assessment Test component, there are 25 marks.
- The first test will be administered after 40-50% of the syllabus has been covered, and the second test will be administered after 85-90% of the syllabus has been covered
- Any two assignment methods mentioned in the 22OB2.4, if an assignment is project-based then only one assignment for the course shall be planned. The teacher should not conduct two assignments at the end of the semester if two assignments are planned.
- For the course, CIE marks will be based on a scaled-down sum of two tests and other methods of assessment.

Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester-End Examination:

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (**duration 03 hours).**

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
3. The students have to answer 5 full questions, selecting one full question from each module.
4. Marks scored shall be proportionally reduced to 50 marks

Suggested Learning Resources:

Text Books

1) Principles of Management – P.C Tripathi, P.N Reddy, McGraw Hill Education, 6th Edition, 2017. ISBN-13:978-93-5260-535-4.
2) Entrepreneurship Development Small Business Enterprises- Poornima M Charantimath,2nd Edition, Pearson Education 2018, ISBN 978-81-317-6226-4.

Reference Books

1) Essentials of Management: An International, Innovation and Leadership perspective by Harold Koontz, Heinz Weihrich McGraw Hill Education, 10th Edition 2016. ISBN- 978-93-392-2286-4.

Web links and Video Lectures (e-Resources):

- https://nptel.ac.in/courses/110107094
- https://nptel.ac.in/courses/110106141
- https://nptel.ac.in/courses/122106031

Activity Based Learning (Suggested Activities in Class)/ Practical Based learning

- Quizzes,
- Assignments,
- Seminars

SIGNALS AND DSP			
IPCC Course Code	**BEE 502**	CIE Marks	50
Teaching Hours/Week (L:T:P: S)	3:0:2:0	SEE Marks	50
Total Hours of Pedagogy	40 hours Theory + 12 Lab slots	Total Marks	100
Credits	04	Exam Hours	03

Course objectives:

1. To explain basic signals, their classification, basic operations on signals, sampling of analog signals, and the properties of the systems.
2. To explain the convolution of signals in continuous and discrete time domain and the properties of impulse response representation.
3. To explain the computation of Discrete Fourier Transform of a sequence by direct method, Linear transformation Method and using Fast Fourier Transformation Algorithms.
4. To explain design of IIR all pole analog filters and transform them into digital filter using Impulse Invariant and Bilinear transformation Techniques and to obtain their Realization.
5. To explain design of FIR filters using Window Method and Frequency Sampling Method and to obtain their Realization.

Teaching-Learning Process (General Instructions)

These are sample Strategies; which teachers can use to accelerate the attainment of the various course outcomes.

1. Lecturer method (L) needs not to be only traditional lecture method, but alternative effective teachingmethods could be adopted to attain the outcomes.
2. Use of Video/Animation to explain functioning of various concepts.
3. Encourage collaborative (Group Learning) Learning in the class.
4. Ask at least three HOT (Higher order Thinking) questions in the class, which promotes critical thinking.
5. Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop design thinkingskills such as the ability to design, evaluate, generalize, and analyse information rather than simply recall it.
6. Introduce Topics in manifold representations.
7. Show the different ways to solve the same problem with different circuits/logic and encourage the studentsto come up with their own creative ways to solve them.
8. Discuss how every concept can be applied to the real world - and when that's possible, it helps improve

the students' understanding.

MODULE-1

Signals, systems and signal processing, classification of signals, Basic Operations on Signals, Basic Elementary Signals, properties of systems. concept of frequency in continuous and Discrete time signals, sampling of analog signals, the sampling theorem , quantization of continuous amplitude and sinusoidal signals , coding of quantized samples, digital to analog conversion,

Time-domain representations for LTI systems: Convolution, impulse response representation, Convolution Sum and Convolution Integral, properties of impulse response representation, solution of difference equations.

Teaching-Learning Process	Chalk and Board, Power Point Presentation, You Tube Videos.

MODULE-2	
Discrete Fourier Transforms (DFT): Introduction to DFT, definition of DFT and its inverse, matrix relation to find DFT and IDFT ,Properties of DFT, linearity, circular time shift, circular frequency shift, circular folding, symmetry of : real valued sequences, real even and odd sequences, DFT of complex conjugate sequence, multiplication of two DFTs- the circular convolution, Parseval's theorem, circular correlation, Digital linear filtering using DFT. Signal segmentation , overlap-save and overlap-add method.	
Teaching-Learning Process	Chalk and Board, Power Point Presentation, You Tube Videos.
MODULE-3	
Fast-Fourier-Transform (FFT) algorithms: Direct computation of DFT, need for efficient computation of the DFT (FFT algorithms)., speed improvement factor, Radix-2 FFT algorithm for the computation of DFT and IDFT–decimation-in-time and Decimation-in-frequency algorithms , calculation of DFT when N is not a power of 2.	
Teaching-Learning Process	Chalk and Board, Power Point Presentation, You Tube Videos.
MODULE-4	
IIR filter design: Classification of analog filters, generation of Butterworth polynomials, frequency transformations. Design of Butterworth filters, low pass, high pass, band pass and band stop filters, Generation of Chebyshev polynomials, design of Chebyshev filters, design of Butterworth and Chebyshev filters using bilinear transformation and Impulse invariance method, representation of IIR filters using direct form one and two, series form and parallel form.	
Teaching-Learning Process	Chalk and Board, Power Point Presentation, You Tube Videos.
MODULE 5	
FIR filter design: Introduction to FIR filters, symmetriv and antisymmetric FIR filters, design of linear phase FIR filters using - Rectangular, Bartlett, Hamming, Hanning and Blackman windows, design of FIR differentiators and Hilbert transformers, FIR filter design using frequency sampling Technique. Representation of FIR filters using direct form and lattice structure.	
Teaching-Learning Process	Chalk and Board, Power Point Presentation, You Tube Videos.

Sl. NO	**Experiments**
1	Verification of Sampling Theorem in time and frequency domains
2	Generation of different signals in both continuous and discrete time domains
3	To perform basic operations on given sequences- Signal folding, evaluation of even and odd signals
4	Evaluation of impulse response of a system.

5.	Solution of a difference equation.
6.	Evaluation of linear convolution and circular convolution of given sequences
7	Computation of N- point DFT and IDFT of a given sequence by use of (a) Defining equation; (b) FFT method
8	Evaluation of circular convolution of two sequences using DFT and IDFT approach.
9	Design and implementation of IIR filters to meet given specification (Low pass, high pass, band pass and band reject filters).
10	Design and implementation of FIR filters to meet given specification (Low pass, high pass, band pass and band reject filters) using different window functions.
11	Design and implementation of FIR filters to meet given specification (Low pass, high pass, band pass and band reject filters) using frequency sampling technique.
12	Realization of IIR and FIR filters.
13	**Following experiments to be done using DSP Kit:** a)Obtain the linear convolution of two sequences b)Compare circular convolution of two sequences c)To find N –point DFT of given sequence d)To find impulse response of first and second order system e)Generation of sine wave and standard test signals

Course outcomes (Course Skill Set):

At the end of the course the student will be able to:

(1)Discuss classification and basic operations that can be performed on both continuous and discrete time signals and to understand sampling theorem.

(2)Evaluate Discrete Fourier Transform of a sequence , to understand the various properties of DFT and signal segmentation using overlap and overlap add method.

(3)Evaluate Discrete Fourier Transform of a sequence using decimation in time and decimation in frequency methods.

(4) To design Butterworth and Chebyshev IIR digital filters and to represent the filters using different methods and to represent IIR filter using different methods.

(5)To design FIR filters using windows method and frequency sampling method and to represent FIR filters using direct method and lattice method.

Text Books/Reference Books:

1.Introduction to Digital Signal Processing, Jhonny R. Jhonson, Pearson 1 st Edition, 2016.

2.Digital Signal Processing – Principles, Algorithms, and Applications,Jhon G. Proakis Dimitris G. Manolakis, Pearson, 4 th Edition, 2007.

3. Digital Signal Processing, A.NagoorKani, McGraw Hill, 2nd Edition, 2012.

4. Digital Signal Processing, Shaila D. Apte,Wiley, 2nd Edition, 2009.

5. Digital Signal Processing, Ashok Amberdar, Cengage, 1st Edition, 2007.
6. Digital Signal Processing, Tarun Kumar Rawat, Oxford, 1st Edition, 2015.

Web links and Video Lectures (e-Resources):
1. http://www.freebookcentre.net/Electronics/DSP-Books
2. https://www.electronicsforu.com/special/cool-stuff-misc/8-free-digital-signal-processing-ebooks

MOOCs
1. https://nptel.ac.in/courses/117102060

Assessment Details (both CIE and SEE)
The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

CIE for the theory component of the IPCC (maximum marks 50)
- IPCC means practical portion integrated with the theory of the course.
- CIE marks for the theory component are 25 marks and that for the practical component is 25 marks.
- 25 marks for the theory component are split into 15 marks for two Internal Assessment Tests (Two Tests, each of 15 Marks with 01-hour duration, are to be conducted) and 10 marks for other assessment methods mentioned in 22OB4.2. The first test at the end of 40-50% coverage of the syllabus and the second test after covering 85-90% of the syllabus.
- Scaled-down marks of the sum of two tests and other assessment methods will be CIE marks for the theory component of IPCC (that is for 25 marks).
- The student has to secure 40% of 25 marks to qualify in the CIE of the theory component of IPCC.

CIE for the practical component of the IPCC
- 15 marks for the conduction of the experiment and preparation of laboratory record, and 10 marks for the test to be conducted after the completion of all the laboratory sessions.
- On completion of every experiment/program in the laboratory, the students shall be evaluated including viva-voce and marks shall be awarded on the same day.
- The CIE marks awarded in the case of the Practical component shall be based on the continuous evaluation of the laboratory report. Each experiment report can be evaluated for 10 marks. Marks of all experiments' write-ups are added and scaled down to 15 marks.
- The laboratory test (duration 02/03 hours) after completion of all the experiments shall be conducted for 50 marks and scaled down to 10 marks.
- Scaled-down marks of write-up evaluations and tests added will be CIE marks for the laboratory component of IPCC for 25 marks.
- The student has to secure 40% of 25 marks to qualify in the CIE of the practical component of the IPCC.

SEE for IPCC
Theory SEE will be conducted by University as per the scheduled timetable, with common question

papers for the course (duration 03 hours)

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), should have a mix of topics under that module.
3. The students have to answer 5 full questions, selecting one full question from each module.
4. Marks scored by the student shall be proportionally scaled down to 50 Marks

The theory portion of the IPCC shall be for both CIE and SEE, whereas the practical portion will have a CIE component only. Questions mentioned in the SEE paper may include questions from the practical component.

Power Electronics		Semester	V
Course Code	BEE503	CIE Marks	50
Teaching Hours/Week (L:T:P: S)	4:0:0:0	SEE Marks	50
Total Hours of Pedagogy	50	Total Marks	100
Credits	04	Exam Hours	
Examination type (SEE)	Theory		

Course objectives:

(1) To give an overview of applications power electronics, different types of power semiconductor devices, their switching characteristics.
(2) To explain power diode characteristics, types, their operation and the effects of power diodes on RL circuits.
(3)To explain the techniques for design and analysis of single phase diode rectifier circuits.
(4) To explain different power transistors, their steady state and switching characteristics and imitations.
(5) To explain different types of Thyristors, their gate characteristics and gate control requirements.
(6)To explain the design, analysis techniques, performance parameters and characteristics of controlled rectifiers, DC- DC, DC -AC converters and Voltage controllers.

Teaching-Learning Process (General Instructions)

These are sample Strategies, which teachers can use to accelerate the attainment of the various course outcomes.

1 Lecturer method (L) needs not to be only traditional lecture method, but alternative effective teaching methods could be adopted to attain the outcomes.
2 Lectures with discussions, question and answer sessions.
3 Informal quizzes.
4 Use of Video/Animation to explain functioning of various concepts.
5 Encourage collaborative (Group Learning) Learning in the class.
6 Ask at least three HOT (Higher order Thinking) questions in the class, which promotes critical thinking.
7 Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop design thinking skills such as the ability to design, evaluate, generalize, and analyse information rather than simply recall it.
8 Introduce Topics in manifold representations.
9 Show the different ways to solve the same problem with different circuits/logic and encourage the students to come up with their own creative ways to solve them.
10 Discuss how every concept can be applied to the real world - and when that's possible, it helps improve the students' understanding.

Module-1

Introduction: Applications of Power Electronics, Ideal Characteristics of switches Characteristics of practical devices; Specifications of Switches, control characteristics of power devices, Types of Power Electronic Circuits, Peripheral Effects, Intelligent Modules.

Power Diodes: Introduction, Diode Characteristics, Reverse Recovery Characteristics, Power Diode Types, Silicon Carbide Diodes, Silicon Carbide Schottky Diodes, Freewheeling diodes**,** Freewheeling diodes with RL load.

Diode Rectifiers: Introduction, Diode Circuits with DC Source connected to R and RL load, Single-Phase Full-Wave Rectifiers with R load, Single-Phase Full-Wave Rectifier with RL Load.

Module-2

Power Transistors: Introduction, Bipolar Junction Transistors – Steady State Characteristics, Switching Characteristics, Switching Limits, Power MOSFETs – Steady State Characteristics, Switching Characteristics, IGBTs; BJT Base Drive, MOSFET Gate Drive, Isolation of Gate and Base Drives, Pulse transformers and Opto-couplers.

Module-3

Thyristors: Introduction, Thyristor Characteristics, Two-Transistor Model of Thyristor, Thyristor Turn- On, Thyristor Turn-Off, A brief study on Thyristor Types, Series Operation of Thyristors, Parallel Operation of Thyristors, di/dt Protection, dv/dt Protection, Thyristor Firing Circuits, Unijunction Transistor.

Module-4

Controlled Rectifiers: Introduction, Single phase half wave circuit with RL Load, Single phase half wave circuit with RL Load and Freewheeling Diode, Single phase half wave circuit with RLE Load, Single-Phase Full Converters with RLE Load, Single-Phase Dual Converters, Principle of operation of Three- Phase duel Converters.

AC Voltage Controllers: Introduction, Principle of phase control & Integral cycle control, Single-Phase Full-Wave Controllers with Resistive Loads, Single- Phase Full-Wave Controllers with Inductive Loads, Three-Phase Full-Wave Controllers.

Module-5

DC-DC Converters: Introduction, principle of step down chopper with R and RL load; principle of step up chopper with R load, Control strategies, performance parameters, DC-DC converter classification.

DC-AC Converters: Introduction, principle of operation single phase bridge inverters, performance parameters, three phase bridge inverters, voltage control of single phase inverters, Harmonic reductions, Current source inverters.

Course outcome (Course Skill Set)

At the end of the course the student will be able to :

1 To give an overview of applications power electronics, different types of power semiconductor devices, their switching characteristics, power diode characteristics, types, their operation and the effects of power diodes on RL circuits.
2 To explain the techniques for design and analysis of single phase diode rectifier circuits.
3 To explain different power transistors, their steady state and switching characteristics and limitations.
4 To explain different types of Thyristors, their gate characteristics and gate control requirements.
5 To explain the design, analysis techniques, performance parameters and characteristics of controlled rectifiers, DC- DC, DC -AC converters and Voltage controllers.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). The student is declared as a pass in the course if he/she secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

- There are 25 marks for the CIE's Assignment component and 25 for the Internal Assessment Test component.
- Each test shall be conducted for 25 marks. The first test will be administered after 40-50% of the coverage of the syllabus, and the second test will be administered after 85-90% of the coverage of the syllabus. The average of the two tests shall be scaled down to 25 marks
- Any two assignment methods mentioned in the 22OB2.4, if an assignment is project-based then only one assignment for the course shall be planned. The schedule for assignments shall be planned properly by the course teacher. The teacher should not conduct two assignments at the end of the semester if two assignments are planned. Each assignment shall be conducted for 25 marks. (If two assignments are conducted then the sum of the two assignments shall be scaled down to 25 marks)
- The final CIE marks of the course out of 50 will be the sum of the scale-down marks of tests and assignment/s marks.

Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester-End Examination:

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (**duration 03 hours).**

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
3. The students have to answer 5 full questions, selecting one full question from each module.
4. Marks scored shall be proportionally reduced to 50 marks.

Suggested Learning Resources:

Books

Textbook

1 Power Electronics: Circuits Devices and Applications, Mohammad H Rashid, Pearson 4th Edition, 2014.

Reference Books

1 Power Electronics, P.S. Bimbhra, Khanna Publishers, 5th Edition, 2012.
2 Power Electronics: Converters, Applications and Design, Ned Mohan et al, Wiley 3rd Edition, 2014.
3 Power Electronics, Daniel W Hart, McGraw Hill, 1st Edition, 2011.
4 Elements of Power Electronics, Philip T Krein, Oxford, Indian Edition, 2008.

Web links and Video Lectures (e-Resources):

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Activity Based Learning (Suggested Activities in Class)/ Practical Based learning •

Power Electronics Laboratory		Semester	V
Course Code	BEEL504	CIE Marks	50
Teaching Hours/Week (L:T:P: S)	0:0:2:0	SEE Marks	50
Credits	01	Exam Hours	100
Examination type (SEE)	Practical		

Course objectives:

1) To conduct experiments on semiconductor devices to obtain their static characteristics. To study different methods of triggering the SCR
2) To study the performance of single phase controlled full wave rectifier and AC voltage controller with R and RL loads.
3) To control the speed of a DC motor, universal motor and stepper motors.
4) To study single phase full bridge inverter connected to resistive load.

Sl.NO	Experiments
1	Static Characteristics of SCR.
2	Static Characteristics of MOSFET and IGBT.
3	Characteristic of TRIAC.
4	SCR turn on circuit using synchronized UJT relaxation oscillator.
5	SCR digital triggering circuit for a single phase controlled rectifier and ac voltage regulator.
6	Single phase controlled full wave rectifier with R load, R –L load, R-L-E load with and without freewheeling diode.
7	AC voltage controller using TRIAC and DIAC combination connected to R and RL loads.
8	Speed control of DC motor using single phase semi converter.
9	Speed control of stepper motor.
10	Speed control of universal motor using ac voltage regulator.
11	Speed control of a separately excited D.C. Motor using an IGBT or MOSFET chopper.
12	Single phase MOSFET/IGBT based PWM inverter.

Course outcomes (Course Skill Set):

At the end of the course the student will be able to:

1 Obtain static characteristics of semiconductor devices to discuss their performance.
2 Trigger the SCR by different methods
3 Verify the performance of single phase controlled full wave rectifier and AC voltage controller with R and RL loads.
4 Control the speed of a DC motor, universal motor and stepper motors.
5 Verify the performance of single phase full bridge inverter connected to resistive load.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation (CIE):

CIE marks for the practical course are **50 Marks**.

The split-up of CIE marks for record/ journal and test are in the ratio **60:40**.

- Each experiment is to be evaluated for conduction with an observation sheet and record write-up. Rubrics for the evaluation of the journal/write-up for hardware/software experiments are designed by the faculty who is handling the laboratory session and are made known to students at the beginning of the practical session.
- Record should contain all the specified experiments in the syllabus and each experiment write-up will be evaluated for 10 marks.
- Total marks scored by the students are scaled down to **30 marks** (60% of maximum marks).
- Weightage to be given for neatness and submission of record/write-up on time.
- Department shall conduct a test of 100 marks after the completion of all the experiments listed in the syllabus.
- In a test, test write-up, conduction of experiment, acceptable result, and procedural knowledge will carry a weightage of 60% and the rest 40% for viva-voce.
- The suitable rubrics can be designed to evaluate each student's performance and learning ability.
- The marks scored shall be scaled down to **20 marks** (40% of the maximum marks).

The Sum of scaled-down marks scored in the report write-up/journal and marks of a test is the total CIE marks scored by the student.

Semester End Evaluation (SEE):

- SEE marks for the practical course are 50 Marks.
- **SEE shall be conducted by the two examiners. One from the same institute as an internal examiner and another from a different institute as an external examiner, appointed by the university.**
- The examination schedule and names of examiners are informed to the university before the conduction of the examination. These practical examinations are to be conducted between the schedule mentioned in the academic calendar of the University.
- All laboratory experiments are to be included for practical examination.
- (Rubrics) Breakup of marks and the instructions printed on the cover page of the answer script to be strictly adhered to by the examiners. **OR** based on the course requirement evaluation rubrics shall be decided jointly by examiners.
- Students can pick one question (experiment) from the questions lot prepared by the examiners jointly.
- Evaluation of test write-up/ conduction procedure and result/viva will be conducted jointly by examiners.

General rubrics suggested for SEE are mentioned here, writeup-20%, Conduction procedure and result in -60%, Viva-voce 20% of maximum marks. SEE for practical shall be evaluated for 100 marks and scored marks shall be scaled down to 50 marks (however, based on course type, rubrics shall be decided by the examiners)

Change of experiment is allowed only once and 15% of Marks allotted to the procedure part are to be made zero.

The minimum duration of SEE is 02 hours

Suggested Learning Resources:

High Voltage Engineering		Semester	V
Course Code	BEE515A	CIE Marks	50
Teaching Hours/Week (L:T:P: S)	3:0:0	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	03	Exam Hours	
Examination type (SEE)	Theory		

Course objectives:

1. To understand the conduction and breakdown mechanism in gases, liquid and solid dielectrics.
2. To know about generation of high voltages and currents and their measurement.
3. To understand the various types of over voltages phenomenon and protection methods.
4. To discuss non-destructive testing of materials and electric apparatus.
5. To discuss high-voltage testing of electrical equipment

Teaching-Learning Process (General Instructions)

These are sample Strategies, which teachers can use to accelerate the attainment of the various course outcomes.

1. Lecturer method (L) needs not to be only traditional lecture method, but alternative effective teaching methods could be adopted to attain the outcomes.
2. Use of Video/Animation to explain functioning of various concepts.
3. Encourage collaborative (Group Learning) Learning in the class.
4. Ask at least three HOT (Higher order Thinking) questions in the class, which promotes critical thinking.
5. Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop design thinking skills such as the ability to design, evaluate, generalize, and analyze information rather than simply recall it.
6. Introduce Topics in manifold representations.
7. Show the different ways to solve the same problem with different circuits/logic and encourage the students to come up with their own creative ways to solve them.

Discuss how every concept can be applied to the real world-and when that's possible, it helps improve the students' understanding..

Module-1

Introduction: Electric field stress, gas, liquid, solid and composite dielectrics.

Conduction and Breakdown in Gases: Gases as Insulating Media, Collision Process – types of collision, Mobility of ions and electrons. Ionization Processes- Ionization by collision. Townsend's Current Growth Equation--Current Growth in the Presence of primary and Secondary Processes, Townsend's Criterion for Breakdown, Breakdown in Electronegative Gases, Time Lags for Breakdown, Paschen's Law, Corona Discharges.

Conduction and Breakdown in Liquid Dielectrics: purification of liquid dielectrics, Breakdown in Liquid dielectrics. - Suspended particle, bubble and stressed oil volume mechanism.

Conduction and Breakdown in Solid Dielectrics: Intrinsic Breakdown, Electromechanical Breakdown, Thermal Breakdown.

Module-2

Generation of High Direct Current Voltages: Voltage Doubler circuit, Voltage multiplier circuit- Cockcroft Walton circuit, Ripple and voltage drop in multiplier circuit. Vandegraaff generator.

Generation of High Alternating Voltages: Cascade transformers, Resonant transformers, Tesla coil.

Generation of Impulse Voltages and currents: Standard impulse wave, Circuit for producing impulse waves- Analysis of impulse generator RLC circuit, Wave shape control, Marx circuit , Generation of impulse current: standard impulse current wave ,Circuit for producing impulse current wave.

Module-3

Measurement of High DC Voltages and Currents: Measurement of High DC Voltages – Series Resistance micro ammeter, Resistance potential divider, Generating voltmeter.

Measurement of High AC voltages- Series impedance voltmeter, Series capacitance voltmeter, Capacitance potential dividers, Capacitance voltage transformers. Electrostatic voltmeter, series capacitance peak voltmeter (chubb-Fortscue method), Spark gaps for measurement of High dc, ac and Impulse voltages - Spark gap measurements, Factors influencing the spark over voltage of sphere gaps.

Measurement of Impulse Voltages – Resistance potential dividers, capacitance voltage dividers, Mixed R-C potential dividers Peak reading voltmeters for impulse voltages.

Measurement of High DC, AC and impulse Currents - Hall generator, Resistive shunt, Rogowski coils and Magnetic links.

Module-4

Natural Causes for Over voltages

Lightning phenomenon –Charge formation in the clouds, Mechanism of lightning strokes, Mathematical model for lighting, Over voltages due to indirect stroke.

Power frequency Overvoltage – Sudden load rejection, Ferranti effect. Control of over voltages due to switching.

Protection of transmission lines against over voltages- Using shielded or ground wires, Ground rods and counter poise wires, Surge arresters -Protector tubes, Nonlinear element surge arrestor.

Module-5

Non-Destructive Testing of Materials and Electrical Apparatus

Power frequency measurements- Schering bridge for audio frequency, transformer ratio arm bridge. Partial discharge measurements- straight discharge detection, Balance detection.

High Voltage Testing of Electrical Apparatus-Testing of insulators, bushings, circuit breakers, cables. Testing of transformers- Impulse test, Tests on surge arrestors.

Course outcome (Course Skill Set)

At the end of the course the student will be able to:

1. Have detailed knowledge of conduction and breakdown phenomenon in gases, liquids and solid dielectrics.
2. Ability to design and simulate the generation of high voltages and currents
3. Ability to design and analyze the measurement techniques for high voltages and currents
4. Summarize overvoltage phenomenon and protection of electric power systems.
5. Explain non-destructive testing of materials and high-voltage testing of electric apparatus

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). The student is declared as a pass in the course if he/she secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

- There are 25 marks for the CIE's Assignment component and 25 for the Internal Assessment Test component.
- Each test shall be conducted for 25 marks. The first test will be administered after 40-50% of the coverage of the syllabus, and the second test will be administered after 85-90% of the coverage of the syllabus. The average of the two tests shall be scaled down to 25 marks
- Any two assignment methods mentioned in the 22OB2.4, if an assignment is project-based then only one assignment for the course shall be planned. The schedule for assignments shall be planned properly by the course teacher. The teacher should not conduct two assignments at the end of the semester if two assignments are planned. Each assignment shall be conducted for 25 marks. (If two assignments are conducted then the sum of the two assignments shall be scaled down to 25 marks)
- The final CIE marks of the course out of 50 will be the sum of the scale-down marks of tests and assignment/s marks.

Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester-End Examination:

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (**duration 03 hours).**

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
3. The students have to answer 5 full questions, selecting one full question from each module.
4. Marks scored shall be proportionally reduced to 50 marks.

Textbook:

1. High Voltage Engineering M.S. Naidu, V.Kamaraju McGraw Hill 5th Edition, 2013.
2. High Voltage Engineering Wadhwa C.L. New Age International 3rd Edition, 2012

Reference Books:

1. High Voltage Engineering Fundamentals E. Kuffel, W.S. Zaengl, J. Kuffel Newnes 2nd Edition, 2000
2. High-Voltage Test and Measuring Techniques Wolfgang Hauschild • Eberhard Lemke Springer 1st Edition2014
3. High Voltage Engineering Farouk A.M. Rizk CRC Press 1st Edition2014

Web links and Video Lectures (e-Resources):

www.nptel.ac.in
Link of Journals, Magazines, websites and Research Papers
http://digital-library.theiet.org/content/journals/hve 2
https://archive.nptel.ac.in/courses/108/104/108104048

Activity Based Learning (Suggested Activities in Class)/ Practical Based learning

Quizzes, Seminars,
Visit transformer manufacturing industry,
Testing laboratories - CPRI.

Power Electronics for Renewable Energy Systems		Semester	V
Course Code	BEE515B	CIE Marks	50
Teaching Hours/Week (L:T:P: S)	3:0:0:0	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	03	Exam Hours	03
Examination type (SEE)	Theory		

Course objectives:

- To appreciate the advantages of renewable energy sources over conventional energy sources
- To study solar PV systems – stand alone and grid connected - and their maximum power tracking methods
- To study wind energy systems and the electrical machines (DFIG) used in WES
- To study MPPT methods and in WES.
- To study other renewable energy sources- biomass, fuel cells and ocean energy
- To study power electronics converters for PV and WES

Teaching-Learning Process (General Instructions)

These are sample Strategies, which teachers can use to accelerate the attainment of the various course outcomes.

1. Chalk and board
2. PPT

Module-1

Review of Power semiconductor devices: Thyristors, GTOs, POWER MOSFETS, IGBTs, MCTs.

Classification of Energy Sources – Importance of Non-conventional energy sources, Advantages and disadvantages of conventional energy sources, Impacts of renewable energy generation on the environment.

Module-2

Solar PV Systems: Solar PV characteristics, Grid requirement for PV, Power electronic converters used for solar PV, Control techniques, 12-pulse rectifier circuits - high voltage 12-pulse rectifier, and high current 12- pulse rectifier, MPPT, Grid connected and Islanding mode, Grid synchronization, PLLs, battery charging in PV systems.

Module-3

Wind Energy Conversion: Wind Turbine characteristics, Grid requirement for Wind, PMSM and DFIG for wind generators, Power electronic converters for PMSM and DFIG rotor side and stator side converters, Control techniques, MPPT, Grid connected and Islanding mode of operation.

Module-4

Qualitative study of other renewable energy resources: Ocean energy, Biomass energy, Hydrogen energy, Fuel cells: Operating principles and characteristics

Module-5

Power Converters and their control in AC microgrids: Microgrid architecture, AC, Microgrid, AC/DC microgrid, Schematics of solar PV and WT powered DC and DC/AC microgrids, Grid-forming, grid-feeding, current source based grid supporting and voltage source based

grid supporting converters. Grid feeding converters- Droop control with dominant inductive and dominant resistive grids, overview of virtual impedance control, overview of hierarchical control.

Course outcome (Course Skill Set)

At the end of the course, the student will be able to :

1. Describe WES and PV systems
2. Develop MPPT algorithms for PV systems and WES.
3. Design converters for PVS and SES
4. Describe biomass, fuel cells and oceanic energy sources
5. Discuss grid connection issues of renewable energy sources.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). The student is declared as a pass in the course if he/she secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

- There are 25 marks for the CIE's Assignment component and 25 for the Internal Assessment Test component.
- Each test shall be conducted for 25 marks. The first test will be administered after 40-50% of the coverage of the syllabus, and the second test will be administered after 85-90% of the coverage of the syllabus. The average of the two tests shall be scaled down to 25 marks
- Any two assignment methods mentioned in the 22OB2.4, if an assignment is project-based then only one assignment for the course shall be planned. The schedule for assignments shall be planned properly by the course teacher. The teacher should not conduct two assignments at the end of the semester if two assignments are planned. Each assignment shall be conducted for 25 marks. (If two assignments are conducted then the sum of the two assignments shall be scaled down to 25 marks)
- The final CIE marks of the course out of 50 will be the sum of the scale-down marks of tests and assignment/s marks.

Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester-End Examination:

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (**duration 03 hours).**

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
3. The students have to answer 5 full questions, selecting one full question from each module.
4. Marks scored shall be proportionally reduced to 50 marks.

Suggested Learning Resources:

Books

1. Fang Lin Luo, Hong Ye, "Advanced DC/AC Inverters: Applications in Renewable

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Energy" CRC Press.
2. Sudipta Chakraborty, Marcelo G. Simões, William E. Kramer, "Power Electronics for Renewable and Distributed Energy Systems" Springer 2013.

Journal Publications

a. "An Overview of Power Electronics Applications in Fuel Cell Systems: DC and AC Converters" Hindawi Publishing Corporation, Scientific World Journal, Volume 2014, Article ID 103709, 9 pageshttp://dx.doi.org/10.1155/2014/103709
b. J. Rocabert, A. Luna, F. Blaabjerg and P. Rodríguez, "Control of Power Converters in AC Microgrids," in *IEEE Transactions on Power Electronics*, vol. 27, no. 11, pp. 4734-4749, Nov. 2012, doi: 10.1109/TPEL.2012.21993
c. S. P. Bihari *et al.*, "A Comprehensive Review of Microgrid Control Mechanism and Impact Assessment for Hybrid Renewable Energy Integration," in *IEEE Access*, vol. 9, pp. 88942-88958, 2021, doi: 10.1109/ACCESS.2021.3090266.

Web links and Video Lectures (e-Resources):

- www.nptel.ac.in
- https://www.youtube.com/watch?v=FvOAZC8Urcs

Activity Based Learning (Suggested Activities in Class)/ Practical Based learning

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ELECTRIC VEHIVLE FUNDAMENTALS		Semester	V
Course Code	BEE515C	CIE Marks	50
Teaching Hours/Week (L:T:P: S)	2:2:0:0	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	03	Exam Hours	03
Examination type (SEE)	Theory		

Course objectives:

- To understand the concept of electric vehicles.
- To study about the motors & drives for electric vehicles.
- To understand the electronics and sensors in electric vehicles.
- To understand the concept of hybrid vehicles.
- To study about fuel cell for electric vehicles.

Teaching-Learning Process (General Instructions)

These are sample Strategies, which teachers can use to accelerate the attainment of the various course outcomes.

1 Lecturer method (L) needs not to be only traditional lecture method, but alternative effective teaching methods could be adopted to attain the outcomes.
2 Lectures with discussions, question and answer sessions.
3 Informal quizzes.
4 Use of Video/Animation to explain functioning of various concepts.
5 Encourage collaborative (Group Learning) Learning in the class.
6 Ask at least three HOT (Higher order Thinking) questions in the class, which promotes critical thinking.
7 Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop design thinking skills such as the ability to design, evaluate, generalize, and analyse information rather than simply recall it.
8 Introduce Topics in manifold representations.
9 Show the different ways to solve the same problem with different circuits/logic and encourage the students to come up with their own creative ways to solve them.

Discuss how every concept can be applied to the real world - and when that's possible, it helps improve the students' understanding.

Module-1

Introduction to Electric Vehicles : Electric Vehicle – Need - Types – Cost and Emissions – End of life. Electric Vehicle Technology – layouts, cables, components, Controls. Batteries – overview and its types. Battery plug-in and life. Ultra-capacitor, Charging – Methods and Standards. Alternate charging sources – Wireless & Solar.

Module-2

Electric Vehicle Motors: Motors (DC, Induction, BLDC) – Types, Principle, Construction, Control. Electric Drive Trains (EDT) – Series HEDT (Electrical Coupling) – Power Rating Design, Peak Power Source (PPS); Parallel HEDT (Mechanical Coupling) – Torque Coupling and Speed Coupling. Switched Reluctance Motors (SRM) Drives – Basic structure, Drive Convertor, Design.

Module-3

Electronics and Sensor-less control in EV: Basic Electronics Devices – Diodes, Thyristors, BJTs, MOSFETs, IGBTs, Convertors, Inverters. Safety – Risks and Guidance, Precautions, High Voltage safety, Hazard management. Sensors - Autonomous EV cars, Self drive Cars, Hacking; Sensor less – Control methods- Phase Flux Linkage-Based Method, Phase Inductance Based, Modulated Signal Injection, Mutually Induced Voltage-Based, Observer-Based.

Module-4
Hybrid Vehicles: Hybrid Electric vehicles – Classification – Micro, Mild, Full, Plug-in, EV. Layout and Architecture – Series, Parallel and Series-Parallel Hybrid, Propulsion systems and components. Regenerative Braking, Economy, Vibration and Noise reduction. Hybrid Electric Vehicles System – Analysis and its Types, Controls.
Module-5
Fuel Cells for Electric vehicles: Fuel cell – Introduction, Technologies & Types, Obstacles. Operation principles, Potential and I-V curve, Fuel and Oxidation Consumption, Fuel cell Characteristics – Efficiency, Durability, Specific power, Factors affecting, Power design of fuel Cell Vehicle and freeze capacity. Lifetime cost of Fuel cell Vehicle – System, Components, maintenance.
Course outcome (Course Skill Set) At the end of the course, the student will be able to : 1. Describe about working principle of electric vehicles. 2. Explain the construction and working principle of various motors used in electric vehicles. 3. Understand about working principle of electronics and sensor less control in electric vehicles. 4. Describe the different types and working principle of hybrid vehicles. 5. Illustrate the various types and working principle of fuel cells.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). The student is declared as a pass in the course if he/she secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

- There are 25 marks for the CIE's Assignment component and 25 for the Internal Assessment Test component.
- Each test shall be conducted for 25 marks. The first test will be administered after 40-50% of the coverage of the syllabus, and the second test will be administered after 85-90% of the coverage of the syllabus. The average of the two tests shall be scaled down to 25 marks
- Any two assignment methods mentioned in the 22OB2.4, if an assignment is project-based then only one assignment for the course shall be planned. The schedule for assignments shall be planned properly by the course teacher. The teacher should not conduct two assignments at the end of the semester if two assignments are planned. Each assignment shall be conducted for 25 marks. (If two assignments are conducted then the sum of the two assignments shall be scaled down to 25 marks)
- The final CIE marks of the course out of 50 will be the sum of the scale-down marks of tests and assignment/s marks.

Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester-End Examination:

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (**duration 03 hours).**

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
3. The students have to answer 5 full questions, selecting one full question from each module.
4. Marks scored shall be proportionally reduced to 50 marks.

Suggested Learning Resources:

Books

1. Jack Erjavec and Jeff Arias, "Hybrid, Electric and Fuel Cell Vehicles", Cengage Learning, 2012.
2. Mehrdad Ehsani, Yimin Gao, sebastien E. Gay and Ali Emadi, "Modern Electric, Hybrid Electric and Fuel Cell Vehicles: Fundamentals, Theory and Design", CRC Press, 2009.

Web links and Video Lectures (e-Resources):

- https://archive.nptel.ac.in/courses/108/106/108106170/

Activity Based Learning (Suggested Activities in Class)/ Practical Based learning

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FUNDAMENTALS OF VLSI DESIGN		Semester	V
Course Code	BEE515D	CIE Marks	50
Teaching Hours/Week (L:T:P: S)	3:0:0:0	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	03	Exam Hours	03
Examination nature (SEE)	Theory		

Course objectives:

Impart knowledge of mass transistors theory and CMOS technology.

- Understand the basic electrical properties of mass and BICMOS circuits.
- Cultivate the concept of subsystem design and layout processes .
- Understand the concept of design process computational elements.

Teaching-Learning Process (General Instructions)

These are sample Strategies, which teachers can use to accelerate the attainment of the various course outcomes.

1 Lecturer method (L) needs not to be only traditional lecture method, but alternative effective teaching methods could be adopted to attain the outcomes.
2 Lectures with discussions, question and answer sessions.
3 Informal quizzes.
4 Use of Video/Animation to explain functioning of various concepts.
5 Encourage collaborative (Group Learning) Learning in the class.
6 Ask at least three HOT (Higher order Thinking) questions in the class, which promotes critical thinking.
7 Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop design thinking skills such as the ability to design, evaluate, generalize, and analyse information rather than simply recall it.
8 Introduce Topics in manifold representations.
9 Show the different ways to solve the same problem with different circuits/logic and encourage the students to come up with their own creative ways to solve them.
10. Discuss how every concept can be applied to the real world - and when that's possible, it helps improve the students' understanding.

Module-1

Moore's law, speed power performance, nMOS fabrication, CMOS fabrication: n-well, p-well processes, BiCMOS, Comparison of bipolar and CMOS.

Basic Electrical Properties of MOS And BiCMOS Circuits: Drain to source current versus voltage characteristics, threshold voltage, transconductance.

Module-2

Basic Electrical Properties of MOS And BiCMOS Circuits: nMOS inverter, Determination of pull up to pull downratio, nMOS inverter driven through one or more pass transistors, alternative forms of pull up, CMOS inverter,BiCMOS inverters, latch up.

Basic Circuit Concepts: Sheet resistance, area capacitance calculation, Delay unit, inverter delay, estimation ofCMOS inverter delay, driving of large capacitance loads, super buffers, BiCMOS drivers.

Module-3

MOS and BiCMOS Circuit Design Processes: MOS layers, stick diagrams, nMOS design style, CMOS design style, design rules and layout, λ - based design.

Scaling of MOS Circuits: scaling factors for device parameters, limitations of scaling.

Module-4
Subsystem Design and Layout-1 : Switch logic pass transistor, Gate logic inverter, NAND gates, NOR gates,pseudo nMOS, Dynamic CMOS, example of structured design, Parity generator, Bus arbitration, multiplexers, logicfunction block, code converter. **Subsystem Design and Layout-2 :** Clocked sequential circuits, dynamic shift registers, bus lines, subsystem designprocesses, General considerations, 4-bit arithmetic processes, 4-bit shifter.
Module-5
Design Process-Computational Elements: Regularity, design of ALU subsystem, ALU using adders, carry lookahead adders, Multipliers, serial parallel multipliers, Braun array, Bough – Wooley multiplier. **Memory, Registerand Aspects of Timing:** Three Transistor Dynamic RAM cell, Dynamic memory cell, Pseudo- Static RAM, JK Flipflop,D Flip-flop circuits, RAM arrays, practical aspects and testability: Some thoughts of performance, optimizationand CAD tools for design and simulation
Course outcome (Course Skill Set) At the end of the course, the student will be able to : 1. Identify the CMOS layout levels, and the design layers used in the process sequence. 2. Describe the general steps required for processing of CMOS integrated circuits. 3. Design static CMOS combinational and sequential logic at the transistor level. 4. Demonstrate different logic styles such as complementary CMOS logic, pass-transistor Logic, dynamic logic, etc. 5. Interpret the need for testability and testing methods in VLSI

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

- For the Assignment component of the CIE, there are 25 marks and for the Internal Assessment Test component, there are 25 marks.
- The first test will be administered after 40-50% of the syllabus has been covered, and the second test will be administered after 85-90% of the syllabus has been covered
- Any two assignment methods mentioned in the 22OB2.4, if an assignment is project-based then only one assignment for the course shall be planned. The teacher should not conduct two assignments at the end of the semester if two assignments are planned.
- For the course, CIE marks will be based on a scaled-down sum of two tests and other methods of assessment.

Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester-End Examination:

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (**duration 03 hours).**

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
3. The students have to answer 5 full questions, selecting one full question from each module.
4. Marks scored shall be proportionally reduced to 50 marks

Suggested Learning Resources:

Books

1. Basic VLSI Design -3rd Edition, Douglas A Pucknell, KamaranEshraghian, Prentice Hall of India publication, 2005.
2. CMOS Digital Integrated Circuits, Analysis And Design, 3rd Edition, Sung – Mo (Steve) Kang, Yusuf Leblbici, Tata McGraw Hill, 2002.
3. VLSI Technology - S.M. Sze, 2nd edition Tata McGraw Hill, 2003.

Web links and Video Lectures (e-Resources):

. .VTU e-shikshanaprogramme VTU Edu-sat programmes • https://nptel.ac.in/courses/117101058
Activity Based Learning (Suggested Activities in Class)/ Practical Based learning • Quizzes • Assignment • Seminars

POWER SYSTEM ANALYSIS I		Semester	VI
Course Code	**BEE601**	CIE Marks	50
Teaching Hours/Week (L:T:P: S)	3:0:2:0	SEE Marks	50
Total Hours of Pedagogy	40 hours Theory + 10 Lab slots	Total Marks	100
Credits	04	Exam Hours	03
Examination nature (SEE)	Theory		

Course objectives:

- To introduce the per unit system and explain its advantages and computation and explain the concept of single line (one line) diagram and its implementation in problems.
- To explain analysis of three phase symmetrical faults on synchronous machine and simple power systems.
- To explain symmetrical components, their advantages and the calculation of symmetrical components of voltages and currents in un-balanced three phase circuits.
- To explain the concept of sequence impedance and sequence networks in three phase unbalanced circuits.
- To explain the analysis of synchronous machine and simple power systems for different unsymmetrical faults using symmetrical components.
- Discuss stability and types of stability for a power system and the equal area criterion for the evaluation of stability of a simple system.

Teaching-Learning Process (General Instructions)
These are sample Strategies; that teachers can use to accelerate the attainment of the various course outcomes.

1. Lecture method (L) need not to be only traditional lecture method, but alternative effective teaching methods could be adopted to attain the outcomes.
2. Use of Video/Animation to explain function for various concepts.
3. Encourage collaborative (Group Learning) Learning in the class.
4. Ask at least three HOT (Higher order Thinking) questions in the class, which promotes critical thinking.
5. Adopt Problem Based Learning (PBL), which foster students 'Analytical skills, develop design thinking skill such as the ability to design, evaluate, generalize, and analyse information rather than simply recall it.
6. Introduce Topics in manifold representations.
7. Show the different ways to solve the same problem with different circuits/logic and encourage the students to come up with their own creative ways to solve them.
8. Discuss how every concept can be applied to the real world-and when that's possible, it will improve the students understanding.

MODULE-1

Representation of Power System Components: Introduction, Single-phase Representation of Balanced Three Phase Networks, One-Line Diagram and Impedance or Reactance Diagram, Per Unit (PU)System, Steady State Model of Synchronous Machine, Power Transformer, Transmission of Electrical Power, Representation of Loads.

MODULE-2

Symmetrical Fault Analysis: Introduction, Transient on transmission Line, Short Circuit of a Synchronous Machine (On No Load), Short Circuit of a Loaded Synchronous Machine, Illustrative simple examples on power systems. Selection of Circuit Breakers.
MODULE-3
Symmetrical Components: Introduction, Symmetrical Component Transformation, Phase Shift in Star-Delta Transformers, Sequence Impedances of Transmission Lines, Sequence Impedances and Sequence Network of Power System, Sequence Impedances and Networks of Synchronous Machine, Sequence Impedances of Transmission Lines, Sequence Impedances Transformers and Construction of Sequence Networks of a Power System.
MODULE-4
Unsymmetrical Fault Analysis: Introduction, Symmetrical Component Analysis of Unsymmetrical Faults, Single Line-To-Ground(LG)Fault, Line-To-Line(LL)Fault, Double Line-To-Ground(LLG)Fault, Open Conductor Faults.
MODULE-5
Power System Stability: Introduction, Dynamics of a Synchronous Machine, Review of Power Angle Equation, Simple Systems, Steady State Stability, Transient Stability, Equal Area Criterion.

PRACTICAL COMPONENT OF IPCC

Sl.NO	Experiments
1	Write a program to draw power angle curves for salient and non-salient pole synchronous machines, reluctance power, excitation, EMF and regulation.
2	Write a program to calculate Sag of a transmission line for i)Poles at equal height ii)Poles at unequal height
3	Write a program to determine the efficiency, Regulation, ABCD parameters for short and long transmission line and verify AD-BC=1.
4	Write a program to determine the efficiency, Regulation and ABCD parameters for medium transmission line for i) Π- configuration ii) T- Configuration and verify AD-BC=1.
5	Write a program to calculate sequence components of line voltages given the unbalanced phase voltages.
6	Write a program to calculate the sequence components of line currents, given the unbalanced phase currents in a three phase i) 3-wire system ii) 4 wire system.
7	Determination of fault currents and voltages in a single transmission line for i) Single Line to Ground Fault. ii)Line to Line Fault iii) Double Line to Ground Fault Using suitable simulating software package.
8	Determination of fault currents and voltages in a single transmission line for Three phase Fault Using suitable simulating software package.
9	Write a program to obtain critical disruptive voltage for various atmospheric and conductor conditions.
10	Write a program to evaluate transient stability of single machine connected to infinite bus.

Course outcomes (Course Skill Set):

At the end of the course, the student will be able to:

1. Model the power system components &construct per unit impedance diagram of power system.
2. Analyse three phase symmetrical faults on power system.
3. Compute unbalanced phasors in terms of sequence components and vice versa, also develop sequence networks.
4. Analyse various unsymmetrical faults on power system.
5. Examine dynamics of synchronous machine and determine the power system stability.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). The student is declared as a pass in the course if he/she secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

The IPCC means the practical portion integrated with the theory of the course. CIE marks for the theory component are **25 marks** and that for the practical component is **25 marks**.

CIE for the theory component of the IPCC

- 25 marks for the theory component are split into **15 marks** for two Internal Assessment Tests (Two Tests, each of 15 Marks with 01-hour duration, are to be conducted) and **10 marks** for other assessment methods mentioned in 22OB4.2. The first test at the end of 40-50% coverage of the syllabus and the second test after covering 85-90% of the syllabus.

- Scaled-down marks of the sum of two tests and other assessment methods will be CIE marks for the theory component of IPCC (that is for **25 marks)**.
- The student has to secure 40% of 25 marks to qualify in the CIE of the theory component of IPCC.

CIE for the practical component of the IPCC

- **15 marks** for the conduction of the experiment and preparation of laboratory record, and **10 marks** for the test to be conducted after the completion of all the laboratory sessions.
- On completion of every experiment/program in the laboratory, the students shall be evaluated including viva-voce and marks shall be awarded on the same day.
- The CIE marks awarded in the case of the Practical component shall be based on the continuous evaluation of the laboratory report. Each experiment report can be evaluated for 10 marks. Marks of all experiments' write-ups are added and scaled down to **15 marks**.
- The laboratory test **(duration 02/03 hours)** after completion of all the experiments shall be conducted for 50 marks and scaled down to **10 marks.**
- Scaled-down marks of write-up evaluations and tests added will be CIE marks for the laboratory component of IPCC for **25 marks**.
- The student has to secure 40% of 25 marks to qualify in the CIE of the practical component of the IPCC.

SEE for IPCC

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (**duration 03 hours**)

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
3. The students have to answer 5 full questions, selecting one full question from each module.
4. Marks scored by the student shall be proportionally scaled down to 50 Marks

The theory portion of the IPCC shall be for both CIE and SEE, whereas the practical portion will have a CIE component only. Questions mentioned in the SEE paper may include questions from the practical component.

- The minimum marks to be secured in CIE to appear for SEE shall be 10 (40% of maximum marks-25) in the theory component and 10 (40% of maximum marks -25) in the practical component. The laboratory component of the IPCC shall be for CIE only. However, in SEE, the questions from the laboratory component shall be included**.** The maximum of 04/05 sub-questions are to be set from the practical component of IPCC, the total marks of all questions should not be more than 20 marks.
- SEE will be conducted for 100 marks and students shall secure 35% of the maximum marks to qualify for the SEE. Marks secured will be scaled down to 50.
- The student is declared as a pass in the course if he/she secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Suggested Learning Resources:

Textbook

1. Modern Power System, D. P. Kothari, McGraw Hill, 4th Edition, 2011.

Reference Books

1. Elements of Power System, William D. Stevenson Jr, McGraw Hill, 4th Edition, 1982.
2. Power System Analysis and Design, J. Duncan Gloveretal, Cengage, 4th Edition, 2008.
3. Power System Analysis, Hadi Sadat, McGraw Hill,1stEdition,2002.

Web links and Video Lectures (e-Resources):
https://nptel.ac.in/courses/108104051

Activity Based Learning (Suggested Activities in Class)/ Practical Based learning

Activity Based Learning, Quizzes, Seminars.

B.E ELECTRICALANDELECTRONICSENGINEERING(EEE)
CHOICE BASED CREDIT SYSTEM (CBCS)
SEMESTER-VI

CONTROLSYSTEMS (PCC)

Subject Code	BEE602	IA Marks	50
Number of Lecture Hours/Week	03:02:00:00	Exam Hours	03
Total Number of Lecture Hours	50	Exam Marks	50

Credits-04

Course objectives:

(1)To analyze and model electrical and mechanical system using analogous systems.
(2) To formulate transfer functions using block diagram and signal flow graphs.
(3) To analyze the transient and steady state time response.
(4) To illustrate the performance of a given system in time and frequency domains, stability analysis using Root locus and Bode plots.
(5) To discuss stability analysis using Nyquist plots, Design controller and compensator for a given specification.

Module-1

Introduction to control systems: Introduction, classification of control systems.
Mathematical models of physical systems: Modeling of mechanical system elements, electrical systems, Analogous systems, Transfer function, Single input single output systems, Procedure for Deriving transfer functions, servomotors, gear trains.

Revised Bloom's Taxonomy Level	L_1–Remembering, L_2–Understanding, L_3–Applying, L_4–Analysing.

Module-2

Block diagram: Elements of Block Diagram, Block diagram of a closed loop system, Block diagram reduction techniques, procedure for block diagram reduction to find transfer function. Numerical.
Signal flow graphs: Construction of signal flow graphs, definition of some important terms, basic properties of signal flow graph, Mason's gain formula, signal flow graph algebra, Numerical

Revised Bloom's Taxonomy Level	L_1–Remembering,L_2–Understanding,L_3–Applying,L_4–Analysing.

Module-3

Time Domain Analysis: Introduction**,** Standard test signals, time response of first order systems, time response of second order systems, Time response specifications, steady state errors and error constants, Approximation of higher order systems and step response of second order systems with zero's.
Routh Stability criterion: BIBO stability, Necessary conditions for stability, Routh stability criterion, difficulties in formulation of Routh table, application of Routh stability criterion to linear feedback systems, relative stability analysis. Numerical

RevisedBloom's TaxonomyLevel	L_2–Understanding,L_3–Applying,L_4–Analysing,L_5–Evaluating.

Module-4

Root locus : Introduction, root locus concepts, construction of root loci, rules for the construction of root locus. Numerical
Frequency domain analysis: Introduction, Co-relation between time and frequencyresponse– 2^{nd}order systems only.
Bode plots: Basic factors G(iw)/H(jw), General procedure for constructing Bode plots, computation of gain margin and phase margin. Numerical

Revised Bloom's Taxonomy Level	L_1–Remembering, L_2–Understanding, L_3–Applying, L_4–Analysing.

Module-5

Control Systems – Compensators and Controllers: Introduction, Phase-Lead Compensator, Phase-Lag Compensator, Lead-Lag Compensator. Proportional controller, Derivative controller, Integral controller, PD Controller, PI Controller, PID Controller,
State space model- Concepts of State, State variable and State model, State Model for linear continuous time systems, Transfer Function from State Space Model, State Transition Matrix and its Properties, Solution of state equation.

RevisedBloom's TaxonomyLevel	L_1–Remembering, L_2–Understanding, L_3–Applying, L_4–Analysing.

Course out comes:

At the end of the course the student will be able to:

1. Analyze and model electrical and mechanical system using analogous.
2. Formulate transfer functions using block diagram and signal flow graphs.
3. Analyze the stability of control system, ability to determine transient and steady state time response.
4. Illustrate the performance of a given system in time and frequency domains, stability analysis using Root locus and Bode plots.
5. Discuss controllers and various compensators.

Graduate Attributes (As per NBA)

Engineering Knowledge, Problem analysis, Modern Tool Usage, Life-long learning.

Question paper pattern:

- The question paper will have ten full questions carrying equal marks. Each full question consisting of 20 marks.
- There will be two full questions from each module.
- Each full question will have sub question covering all the topics under a module.
- The students will have to answer five full questions, selecting one full question from each module.

Textbook

1	Control Systems	Anand Kumar	PHI	2nd Edition,2014

Reference Books

1	Automatic Control Systems	Farid Golnaraghi, Benjamin C.Kuo	Wiley	9th Edition,2010
2	Control Systems Engineering	Norman S.Nise	Wiley	4th Edition,2004
3	Modern Control Systems	Richard C D orfetal	Pearson	11th Edition,2008
4	Control Systems, Principles and Design	M.Gopal	McGawHill	4th Edition,2012
5	Control Systems Engineering	S.Salivahananetal	Pearson	1st Edition,2015

Medium Voltage Substation Design		Semester	VI
Course Code	BEE613A	CIE Marks	50
Teaching Hours/Week (L:T:P: S)	3:0:0:0	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	03	Exam Hours	03
Examination type (SEE)	Theory		

Course objectives:

- Explain the concepts behind substation engineering and design.
- Demonstrate how to prepare and read SLD for substation.
- Demonstrate how to size and select LV and HV equipment's for power distribution, protection and switchgear.
- Formulate and analyze erection key diagram, layout preparation and necessary sectional clearance in substation installation.
- Assess multi-disciplinary approach in substation erection.

Teaching-Learning Process (General Instructions)

These are sample Strategies, which teachers can use to accelerate the attainment of the various course outcomes.

1. Chalk and Talk,
2. Discussion and Q & A
3. Quizzes
4. Videos and E –resources
5. Substation Visits etc

Module-1

Substation Basics

Substation Introduction and Classifications, Busbar Types in Outdoor Switchyard, Outdoor /Indoor Substation - Auxiliary Equipment in a Substation, Standards and Practices, Factors Influencing Substation Design -Different factors like Altitude, Ambient Temperature etc. with animation, Selection of Dielectric Strength for Electrical Equipment with animation on creepage distance, Testing of Electrical Equipment, Concepts of Single Line Diagram.

Module-2

Transformers and Switchgears

Classification of Transformers with a practical overview, Transformer Percentage Impedance and Losses, Construction including busbar arrangement and safety features, Classifications of MV Switchgear and Key Design Parameters, MV Switchgear Construction, LV Compartment, Security Interlocks & General Arrangement, Control Circuit Components - Control Relays, Time Delay Relays & Latched Relays), Control Scheme Basics, Trip Lockout, TCS and Anti-pumping Circuits, Logic Schemes.

Module-3

Protection and Station Auxiliary equipment and Digital Substation

Power System Network, Protection System, Overcurrent and Earth Fault, Overcurrent and Earth Fault – Coordination. Distribution Feeder Protection, Transformer – Unit/Main Protection, Transformer Protection, Familiarization of NUMERICAL Relays, Diesel Generator System, Instrument transformers (CT), Basics of AC/DC Auxiliary Power System & Sizing of Aux. Transformer, DC System Components, Battery Sizing & charger Sizing, DG Set Classification, and sizing. Evolution of Substation Automation, Communication System Fundamentals, Substation Automation System: DI, DO, AI, AO, Remote Terminal Unit –

RTU, Substation Automation Requirements – Time Synchronizing, HMI, SCADA.

Module-4

Cabling System & Illumination, Outdoor SS Layout engineering, Erection Key Diagram, Earthing and Lighting Protection

LV Cables - Power & Control, MV Cables, Methods for Cable Installation, Practical aspects of Cable Sizing, Cable Glands, Lugs, and their Accessories, Types and Classifications of Surge Arresters, Characteristics of Surge Arresters, Illumination System Design, Equipment Layout engineering aspects for Outdoor Substation and related calculations and guide lines, Basics of Outdoor Air Insulated Substation up to 33 kV - Statutory Clearances, Practical approach to Cable routing layout for Outdoor S/S, Practical approach to Erection Key Diagram (EKD) for outdoor switchyard, Importance and Types of Earthing, Earthing Design, Types of Earthing Material, Lightning Protection.

Module-5

MV substation Civil design, Fire Protection, HVAC, Maintenance and Safety

Transformer Foundation, Fire Wall, and Fire Rated Doors, Civil & Structural Engineering - MV SS, Fire Detection & Alarm System and Fire Suppression System, Heating, Ventilation and Air-conditioning (HVAC) for Substation, Need for Maintenance of a Substation & schedule, Electrical Safety Rules, Standard Operating Procedures.

Course outcome (Course Skill Set)

At the end of the course, the student will be able to :

1. Explain the key concepts of design, construction, operation, and maintenance of electrical substations.
2. Develop design calculations in substation engineering such as earth-mat, lightning protection, earthing, lighting, and cable sizing.
3. Develop design calculation for sizing of power transformers, diesel generator.
4. Select LV and HV equipment's in substation for power distribution, protection, and switchgear.
5. Explain Electrical Safety Rules, SOPs.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). The student is declared as a pass in the course if he/she secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

- There are 25 marks for the CIE's Assignment component and 25 for the Internal Assessment Test component.
- Each test shall be conducted for 25 marks. The first test will be administered after 40-50% of the coverage of the syllabus, and the second test will be administered after 85-90% of the coverage of the syllabus. The average of the two tests shall be scaled down to 25 marks
- Any two assignment methods mentioned in the 22OB2.4, if an assignment is project-based then only one assignment for the course shall be planned. The schedule for assignments shall be planned properly by the course teacher. The teacher should not conduct two assignments at the end of the semester if two assignments are planned. Each assignment shall be conducted for 25 marks. (If two assignments are conducted then the sum of the two assignments shall be scaled down to 25 marks)
- The final CIE marks of the course out of 50 will be the sum of the scale-down marks of tests and assignment/s marks.

Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester-End Examination:

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (**duration 03 hours).**

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
3. The students have to answer 5 full questions, selecting one full question from each module.
4. Marks scored shall be proportionally reduced to 50 marks.

Suggested Learning Resources:

Books

1. Partap Singh Satnam, P.V. Gupta, "Sub-station Design and Equipment", Dhanpat Rai Publications, 1 st Edition, 2013
2. Sunil S. Rao, "Switchgear Protection and Power Systems (Theory, Practice & Solved Problems)", Khanna Publications, 14th Edition, 2019.
3. Electrical substation and engineering & practice by S. Rao, Khanna Publishers 2015
4. McDonald John D, "Electric Power Substations Engineering," CRC Press, 3 rd. Edition, 2012

Web links and Video Lectures (e-Resources):

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Activity Based Learning (Suggested Activities in Class)/ Practical Based learning •

EMBEDDED SYSTEM DESIGN		Semester	VI
Course Code	**BEE613B**	CIE Marks	50
Teaching Hours/Week (L:T:P: S)	3:0:0:0	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	03	Exam Hours	03
Examination nature (SEE)	Theory		

Course objectives:

To teach students

- Introductory topics of Embedded System design
- Characteristics & attributes of Embedded System
- Introduction of Embedded System Software and Hardware development
- RTOS based Embedded system design

Teaching-Learning Process (General Instructions)

These are sample Strategies, which teachers can use to accelerate the attainment of the various course outcomes.

. These are sample Strategies, which teacher can use to accelerate the attainment of the various course
outcomes and make Teaching –Learning more effective

1. Lecturer method (L) does not mean only the traditional lecture method, but a different type of teaching method may be adopted to develop the outcomes.
2. Show Video/animation films to explain the functioning of various analog and digital circuits.
3. Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop thinking skills such as the ability to evaluate, generalize, and analyse information rather than simply recall it.
4. Show the different ways to solve the same problem and encourage the students to come up with their own creative ways to solve them.
5. Discuss how every concept can be applied to the real world - and when that's possible, it helps improve the students' understanding

Module-1

Introduction: Embedded Systems and general purpose computer systems, history, classifications, applications and purpose of embedded systems (Chapter 1 – Text 1)
Core of Embedded Systems : Microprocessors and microcontrollers, RISC and CISC controllers, Big endian and Little endian processors, Application specific ICs, Programmable logic devices, COTS, sensors and actuators, communication interface, embedded firmware, other system components, PCB and passive components (Chapter 2 – Text 1)

Module-2

Characteristics and quality attributes of embedded systems: Characteristics, Operational and nonoperational quality attributes, application specific embedded system - washing machine, domain specific – automotive (Chapter 3 & 4 – Text 1)

Module-3

Hardware Software Co design and Program Modelling : Fundamental issues in Hardware Software Co-design, Computational models in Embedded System Design (Chapter 7 – Text 1: 7.1, 7.2)
Embedded Hardware Design and Development: Analog Electronic Components, Digital Electronic Components, VLSI & Integrated Circuit Design, Electronic Design Automation Tools (Chapter 8 – Text 1: 8.1, 8.2, 8.3, 8.4)

Module-4

Embedded Firmware Design and Development: Embedded Firmware Design Approaches, Embedded Firmware Development Languages (Chapter 9 – Text 1: 9.1, 9.2)
Embedded System Development Environments: Types of files generated on cross compilation (only explanation – programming codes need not be dealt), disassemble/decompliler, Simulators, Emulators and Debugging (Chapter 13 – Text 1: 13.2, 13.3,13.4)

Module-5

Real-time Operating System(RTOS) based Embedded System Design: Operating System basics, Types of Operating Systems, Tasks, Process and Threads, Multiprocessing and Multitasking, Task Scheduling (Chapter 10 – Text 1: 10.1 to 10.5)

Course outcome (Course Skill Set)

At the end of the course, the student will be able to :

1. Explain characteristics of Embedded System design
2. Acquire knowledge about basic concepts of circuit emulators, debugging and RTOS
3. Analyse embedded system software and hardware requirements
4. Develop programming skills in embedded systems for various applications
5. Design basic embedded system for real time applications

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

- For the Assignment component of the CIE, there are 25 marks and for the Internal Assessment Test component, there are 25 marks.
- The first test will be administered after 40-50% of the syllabus has been covered, and the second test will be administered after 85-90% of the syllabus has been covered
- Any two assignment methods mentioned in the 22OB2.4, if an assignment is project-based then only one assignment for the course shall be planned. The teacher should not conduct two assignments at the end of the semester if two assignments are planned.
- For the course, CIE marks will be based on a scaled-down sum of two tests and other methods of assessment.

Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester-End Examination:

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (**duration 03 hours).**

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
3. The students have to answer 5 full questions, selecting one full question from each module.
4. Marks scored shall be proportionally reduced to 50 marks

Suggested Learning Resources:

Books

1.Shibu K V, "Introduction to Embedded Systems", Second Edition, McGraw Hill Education

Web links and Video Lectures (e-Resources):
. NPTL Lectures: https://nptel.ac.in/courses/108102045 • Embedded Systems, IIT Delhi, Prof. Santanu Chaudhary
Activity Based Learning (Suggested Activities in Class)/ Practical Based learning To design a simple Embedded System like simple remote ・ To demonstrate simple microcontroller based experiments like LED interfacing, LCD interfacing, DAC etc

FACTS AND HVDC TRANSMISSION		Semester	VI
Course Code	BEE613C	CIE Marks	50
Teaching Hours/Week(L:T:P:S)	(3:0:0)	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	03	Exam Hours	03
Examination type (SEE)	Theory		

Course objectives:

- To discuss transmission interconnections, flow of Power in an AC System, limits of the loading capability, dynamic stability considerations of a transmission interconnection and controllable parameters.
- To explain the basic concepts, definitions of flexible ac transmission systems and benefits from FACTS technology.
- To describe shunt controllers, Static Var Compensator and Static Compensator for injecting reactive power in the transmission system in enhancing the controllability and power transfer capability.
- To describe series Controllers Thyristor-Controlled Series Capacitor (TCSC) and the Static Synchronous Series Compensator (SSSC) for control of the transmission line current.
- To explain advantages of HVDC power transmission, overview and organization of HVDC system.
- To describe the basic components of a converter, the methods for compensating the reactive power demanded by the converter.
- Explain converter control for HVDC systems, commutation failure, control functions.

Teaching-Learning Process (General Instructions)

These are sample Strategies, which teachers can use to accelerate the attainment of the various course outcomes.

1. Lecturer method (L) needs not to be only traditional lecture method, but alternative effective teaching methods could be adopted to attain the outcomes.
2. Use of Video/Animation to explain functioning of various concepts.
3. Encourage collaborative (Group Learning) Learning in the class.
4. Ask at least three HOT (Higher order Thinking) questions in the class, which promotes critical thinking.
5. Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop design thinking skills such as the ability to design, evaluate, generalize, and analyse information rather than simply recall it.
6. Introduce Topics in manifold representations.
7. Show the different ways to solve the same problem with different circuits/logic and encourage the students to come up with their own creative ways to solve them.
8. Discuss how every concept can be applied to the real world - and when that's possible, it helps improve the students' understanding.

Module-1

FACTS Concept and General System Considerations: Transmission Interconnections, Flow of Power in an AC System, What Limits the Loading Capability? Power Flow and Dynamic Stability Considerations of a Transmission Interconnection, Relative Importance of Controllable Parameters, Basic Types of FACTS Controllers, Brief Description and Definitions of FACTS Controllers, Checklist of Possible Benefits from FACTS Technology, In Perspective: HVDC or FACTS.

Module-2

Static Shunt Compensators: Objectives of Shunt Compensation - Midpoint Voltage Regulation for Line Segmentation, End of Line Voltage Support to Prevent Voltage Instability, Improvement of Transient Stability. Methods of Controllable Var Generation –Thyristor controlled Reactor (TCR) and Thyristor Switched Reactor (TSR), Thyristor Switched Capacitor (TSC).Operation of Single Phase TSC – TSR. Switching Converter Type Var Generators, Basic Operating Principles, Basic Control Approaches.

Static VAR Compensators: SVC and STATCOM, the Regulation Slope. Comparison between STATCOM and SVC, V –I and V –Q Characteristics, Transient stability, Response Time.
Module-3
Static Series Compensators: Objectives of Series Compensation, Concept of Series Capacitive Compensation, Voltage Stability, Improvement of Transient Stability. GTO Thyristor-Controlled Series Capacitor, Thyristor-Switched Series Capacitor, Thyristor-Controlled Series Capacitor, The Static synchronous Series Compensator, Transmitted Power Versus Transmission Angle Characteristic.
Module-4
Development of HVDC Technology: Introduction, Advantages of HVDC Systems, HVDC System Costs, Overview and Organization of HVDC Systems, HVDC Characteristics and Economic Aspects. Power Conversion: 3-Phase Converter, 3-Phase Full Bridge Converter, 12-Pulse Converter.
Module-5
Control of HVDC Converter and System: Converter Control for an HVDC System, Commutation Failure, HVDC Control and Design, HVDC Control Functions, Reactive Power and Voltage Stability.

Course outcome(Course Skill Set)

At the end of the course, the student will be able to :

1. Explain the basic concepts, definitions of flexible ac transmission systems and benefits from FACTS technology.
2. Describe shunt controllers, Static Var Compensator and Static Compensator for injecting reactive power in the transmission system in enhancing the controllability and power transfer capability.
3. Describe series Controllers Thyristor-Controlled Series Capacitor (TCSC) and the Static Synchronous Series Compensator (SSSC) for control of the transmission line current.
4. Explain advantages of HVDC power transmission, overview and organization of HVDC system.
5. Explain converter control for HVDC systems, commutation failure, control.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). The student is declared as a pass in the course if he/she secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

- *There are 25 marks for the CIE's Assignment component and 25 for the Internal Assessment Test component.*
- *Each test shall be conducted for 25 marks. The first test will be administered after 40-50% of the coverage of the syllabus, and the second test will be administered after 85-90% of the coverage of the syllabus. The average of the two tests shall be scaled down to 25 marks*
- *Any two assignment methods mentioned in the22OB2.4,if an assignment is project-based then only one assignment for the course shall be planned. The schedule for assignments shall be planned properly by the course teacher. The teacher should not conduct two assignments at the end of the semester if two assignments are planned. Each assignment shall be conducted for 25 marks. (If two assignments are conducted then the sum of the two assignments shall be scaled down to 25 marks)*
- *The final CIE marks of the course out of 50 will be the sum of the scale-down marks of tests and assignment/s marks.*

Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester-End Examination:

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (duration 03 hours).

1. *The question paper will have ten questions. Each question is set for 20 marks.*
2. *There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), should have a mix of topics under that module.*
3. *The students have to answer 5 full questions, selecting one full question from each module.*
4. *Marks scored shall be proportionally reduced to50 marks.*

Suggested Learning Resources:

Books

1. Understanding FACTS: Concepts and Technology of Flexible AC Transmission Systems Narain G Hingorani, Laszlo Gyugyi, Wiley 1st Edition, 2000
2. HVDC Transmission: Power Conversion Applications in Power Systems, Chan-Ki Kim et al, Wiley, 1st Edition, 2009
3. Thyristor Based FACTS Controllers for Electrical Transmission Systems , R. Mohan Mathur, Rajiv K. Varma, Wiley, 1st Edition, 2002

Web links and Video Lectures (e-Resources):

- Courses available through NPTEL. -website: nptel.ac.in

Activity Based Learning (Suggested Activities in Class)/Practical Based learning

- *Quiz*
- *Group discussion*

Electric Motor and Drive Systems for Electric Vehicles		Semester	VI
Course Code	BEE613D	CIE Marks	50
Teaching Hours/Week (L:T:P: S)	3:0:0:0	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	03	Exam Hours	
Examination type (SEE)	Theory		

Course objectives:

Course Objectives :The objective of this course is to make the student

1. Understand the concept of electric vehicles technology
2. Gain knowledge on power requirement of EV
3. Know the performance and control of various motors for EVs

Teaching-Learning Process (General Instructions)

These are sample Strategies, which teachers can use to accelerate the attainment of the various course outcomes.

1. Lecturer method (L) needs not to be only traditional lecture method, but alternative effective teaching methods could be adopted to attain the outcomes.
2. Use of Video/Animation to explain functioning of various concepts.
3. Encourage collaborative (Group Learning) Learning in the class.
4. Ask at least three HOT (Higher order Thinking) questions in the class, which promotes critical thinking.
5. Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop design thinking skills such as the ability to design, evaluate, generalize, and analyse information rather than simply recall it.
6. Introduce Topics in manifold representations.
7. Show the different ways to solve the same problem with different circuits/logic and encourage the students to come up with their own creative ways to solve them.

Discuss how every concept can be applied to the real world - and when that's possible, it helps improve the students' understanding.

Module-1

Introduction -History of Electric and Hybrid Electric Vehicles.

Vehicle Fundamentals-General Description of Vehicle Movement, Power Train Tractive Effort and Vehicle Speed.

Vehicle Performance –Maximum Speed of a Vehicle , Gradeability, Acceleration Performance ,Braking Performance , Braking Force , Braking Distribution on Front and Rear Axles

Module-2

Electric Vehicles:

Configurations of Electric Vehicles, Performance of Electric Vehicles , Traction Motor Characteristics, Tractive Effort and Transmission Requirement , Vehicle Performance , Energy Consumption.

Module-3

DC Motor Drives:

Operating principle, Speed characteristics of DC motors, Combined Armature Voltage and Field Control, Chopper Control of DC Motors.

Control Methods- Two-Quadrant Control **-**Single Chopper with a Reverse Switch, Class C Two-Quadrant Chopper, Four-Quadrant control.

Module-4

Induction Motor Drives:

Basic Operation Principles of Induction Motors , Steady-State Performance Constant v/f Control, Power Electronic Control.

Field Orientation Control(FOC): Principles of FOC.

Control methods- Direction Rotor Flux control, Indirect Rotor Flux control, Voltage Source Inverter control - Voltage Control, Current Control.

Module-5

BLDC Motor Drives:

BLDC Machine Construction and Classification, Performance Analysis, Control of BLDC Motor Drives.

Control Techniques - Methods Using Observers, Methods Using Back EMF Sensing.

Switched Reluctance Motor Drives (SRM)-Basic Magnetic Structure, Torque Production,

Methods of Control -Phase Flux Linkage Method, Mutually Induced Voltage Method, Observer-Based Method, Self-Tuning Using an Artificial Neural Network.

Course outcome (Course Skill Set)

At the end of the course, the student will be able to :

1.Explain the Fundamental and Performance of EV

2. Understand the Characteristics of motor control and energy consumption for EV operation

3.Analyse the Power electronics and sensors in DC motor electric vehicles.

4. Design and Analysethe induction motor drives and discuss methods for controlling them.

5. Comprehend the construction, working principle and controlof BLDC and SRM motors.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). The student is declared as a pass in the course if he/she secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

- There are 25 marks for the CIE's Assignment component and 25 for the Internal Assessment Test component.
- Each test shall be conducted for 25 marks. The first test will be administered after 40-50% of the coverage of the syllabus, and the second test will be administered after 85-90% of the coverage of the syllabus. The average of the two tests shall be scaled down to 25 marks
- Any two assignment methods mentioned in the 22OB2.4, if an assignment is project-based then only one assignment for the course shall be planned. The schedule for assignments shall be planned properly by the course teacher. The teacher should not conduct two assignments at the end of the semester if two assignments are planned. Each assignment shall be conducted for 25 marks. (If two assignments are conducted then the sum of the two assignments shall be scaled down to 25 marks)
- The final CIE marks of the course out of 50 will be the sum of the scale-down marks of tests and assignment/s marks.

Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester-End Examination:

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (**duration 03 hours).**

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
3. The students have to answer 5 full questions, selecting one full question from each module.
4. Marks scored shall be proportionally reduced to 50 marks.

Suggested Learning Resources:

Text Books

1. Modern Electric, Hybrid Electric, and Fuel Cell Vehicles.
Fundamentals, Theory, and Design by Mehrdad Ehsani, Yimin Gao, Sebastien E. Gay, Ali Emadi, CRC Press, 2004.
1. Electric and Hybrid Vehicles Design Fundamentals Third Edition Iqbal Husain, CRC Press

Reference Books:

1. Hybrid ElectricVehicles, Principles And ApplicationsWith Practical Perspectives by Chris Mi , M. Abul Masrur, David Wenzhong Gao John Wiley & Sons, 2011.
2 Electric and Hybrid Vehicles, .T. Denton, Routledge, 2016.
3. Permanent Magnet Synchronous and Brushless DC Motor Drives , R Krishnan, CRC Press
4. Switched Reluctance Motor Drives, Berker B., James W. J. & A. Emadi, CRC Press

Web links and Video Lectures (e-Resources):

NPTEL courses – eMobility and Electric Vehicle Engineering https://archive.nptel.ac.in/courses/108/106/108106182
Activity Based Learning (Suggested Activities in Class)/ Practical Based learning Quizzes, Seminars, visit EV manufacturing industry

Utilization of Electric Power		Semester	VI
Course Code	**BEE654A**	CIE Marks	50
Teaching Hours/Week (L:T:P: S)	3:0:0:0	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	03	Exam Hours	03
Examination type (SEE)	Theory		

Course objectives:

(1) To discuss electric heating, air-conditioning and electric welding.
(2) To explain laws of electrolysis, extraction and refining of metals and electro deposition.
(3) To explain the terminology of illumination, laws of illumination, construction and working of electric lamps.
(4) To explain design of interior and exterior lighting systems- illumination levels for various purposes light fittings- factory lighting- flood lighting-street lighting
(5) To discuss systems of electric traction, speed time curves and mechanics of train movement.
(6) To discuss motors used for electric traction and their control.
(7) To discuss braking of electric motors, traction systems and power supply and other traction systems.
(8) To Give awareness of technology of electric and hybrid electric vehicles.

Teaching-Learning Process (General Instructions)

These are sample Strategies, which teachers can use to accelerate the attainment of the various course outcomes.

1 Lecturer method (L) needs not to be only traditional lecture method, but alternative effective teaching methods could be adopted to attain the outcomes.
2 Use of Video/Animation to explain functioning of various concepts.
3 Encourage collaborative (Group Learning) Learning in the class.
4 Ask at least three HOT (Higher order Thinking) questions in the class, which promotes critical thinking.
5 Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop design thinking skills such as the ability to design, evaluate, generalize, and analyse information rather than simply recall it.
6 Introduce Topics in manifold representations.
7 Show the different ways to solve the same problem with different circuits/logic and encourage the students to come up with their own creative ways to solve them.
8 Discuss how every concept can be applied to the real world - and when that's possible, it helps improve the students' understanding.

Module-1

Heating and welding: Electric Heating, Resistance ovens, Radiant Heating, Induction Heating, High frequency Eddy Current Heating, Dielectric Heating, The Arc Furnace, Heating of Buildings, Air – Conditioning, ElectricWelding, Modern Welding Techniques.

Electrolytic Electro – Metallurgical Process: Ionization, Faraday's Laws of Electrolysis, Definitions, Extraction of Metals, Refining of Metals, Electro Deposition.

Module-2

Illumination: Introduction, Radiant Energy, Definitions, Laws of Illumination, Polar Curves, Photometry,Measurement of Mean Spherical Candle Power by Integrating Sphere, Illumination Photometer, Energy Radiation and luminous Efficiency, electric Lamps, Cold Cathode Lamp, Lighting Fittings, Illumination for Different Purposes, Requirements of Good Lighting.

Module-3

Electric Traction Speed - Time Curves and Mechanics of Train Movement: Introduction, Systems of Traction, Systems of electric Traction, Speed - Time Curves for Train Movement, Mechanics of Train Movement, Train Resistance, Adhesive Weight, Coefficient of Adhesion.

Motors for Electric traction: Introduction, Series and Shunt Motors for Traction Services, Two Similar Motors(Series Type) are used to drive a Motor Car, Tractive Effort and Horse Power, AC Series Motor, Three Phase Induction Motor.

Control of motors: Control of DC Motors, Tapped Field Control or Control by Field Weakening, MultipleUnit Control, Control of Single Phase Motors, Control of Three Phase Motors.

Module-4
Braking: Introduction, Regenerative Braking with Three Phase Induction Motors, Braking with Single Phase Series Motors, Mechanical braking, Magnetic Track Brake, Electro – Mechanical Drum Brakes. **Electric Traction Systems and Power Supply:** System of Electric Traction AC Electrification, Transmission Lines to Sub - Stations, Sub – Stations, Feeding and Distribution System of AC Traction Feeding and Distribution System for DC Tramways, Electrolysis by Currents through Earth, Negative Booster, System of Current Collection, Trolley Wires. **Trams, Trolley Buses and Diesel – Electric Traction:** Tramways, The Trolley – Bus, Diesel Electric Traction.
Module-5
Electric Vehicles: Configurations of Electric Vehicles, Performance of Electric Vehicles, Tractive Effort in Normal Driving, Energy Consumption. **Hybrid Electric Vehicles:** Concept of Hybrid Electric Drive Trains, Architectures of Hybrid Electric Drive Trains.
Course outcome (Course Skill Set) At the end of the course the student will be able to : 1. Discuss different methods of electric heating & welding. 2. Discuss the laws of electrolysis, extraction, refining of metals and electro deposition process. 3. Discuss the laws of illumination, different types of lamps, lighting schemes and design of lighting systems. Analyze systems of electric traction, speed time curves and mechanics of train movement. 4. Explain the motors used for electric traction, their control & braking and power supply system used for electric traction.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). The student is declared as a pass in the course if he/she secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

- There are 25 marks for the CIE's Assignment component and 25 for the Internal Assessment Test component.
- Each test shall be conducted for 25 marks. The first test will be administered after 40-50% of the coverage of the syllabus, and the second test will be administered after 85-90% of the coverage of the syllabus. The average of the two tests shall be scaled down to 25 marks
- Any two assignment methods mentioned in the 22OB2.4, if an assignment is project-based then only one assignment for the course shall be planned. The schedule for assignments shall be planned properly by the course teacher. The teacher should not conduct two assignments at the end of the semester if two assignments are planned. Each assignment shall be conducted for 25 marks. (If two assignments are conducted then the sum of the two assignments shall be scaled down to 25 marks)
- The final CIE marks of the course out of 50 will be the sum of the scale-down marks of tests and assignment/s marks.

Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester-End Examination:

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (**duration 03 hours).**

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
3. The students have to answer 5 full questions, selecting one full question from each module.
4. Marks scored shall be proportionally reduced to 50 marks.

Suggested Learning Resources:

Books

Textbooks

1. A Text Book on Power System Engineering, A. Chakrabarti et al, Dhanpat Rai and Co, 2nd Edition, 2010.
2. Modern Electric, Hybrid Electric, and Fuel Cell Vehicles: Fundamentals Theory, and Design, (Chapters 04and 05 for module 5), Mehrdad Ehsani et al, CRC Press, 1st Edition, 2005.

Reference Books

1. Utilization, Generation and Conservation of Electrical Energy, Sunil S Rao, Khanna Publishers, 1st Edition,2011.
2. Utilization of Electric Power and Electric Traction, G.C. Garg, Khanna Publishers, 9th Edition, 2014.

Web links and Video Lectures (e-Resources):

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Activity Based Learning (Suggested Activities in Class)/ Practical Based learning

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Technologies of Renewable Energy Sources		Semester	VI
Course Code	**BEE654B**	CIE Marks	50
Teaching Hours/Week (L:T:P: S)	3:0:0:0	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	03	Exam Hours	03
Examination type (SEE)	Theory		

Course objectives:

(1) To discuss causes of energy scarcity and its solution, energy resources and availability of renewable energy.
(2) To explain sun – earth geometric relationship, Earth – Sun Angles and their Relationships.
(3) To discuss about solar energy reaching the Earth's surface and solar thermal energy applications.To discuss types of solar collectors, their configurations and their applications.
(4) To explain the components of a solar cell system, equivalent circuit of a solar cell, its characteristicsand applications.
(5) To discuss benefits of hydrogen energy, production of hydrogen energy, storage its advantages and disadvantages.
(6) To discuss wind turbines, wind resources, site selection for wind turbine.
(7) To discuss geothermal systems, their classification and geothermal based electric power generation (9To discuss waste recovery management systems, advantages and disadvantages.
(8) To discuss biomass composition, production, types of biomass gasifiers, properties of producer gas benefits.
(9) To discuss tidal energy resources, energy availability, power generation.
(10) To explain motion in the sea wave, power associated with sea wave and energy availability and the devicesfor harnessing wave energy.

Teaching-Learning Process (General Instructions)

These are sample Strategies, which teachers can use to accelerate the attainment of the various course outcomes.

1 Lecturer method (L) needs not to be only traditional lecture method, but alternative effective teaching methods could be adopted to attain the outcomes.
2 Use of Video/Animation to explain functioning of various concepts.
3 Encourage collaborative (Group Learning) Learning in the class.
4 Ask at least three HOT (Higher order Thinking) questions in the class, which promotes critical thinking.
5 Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop design thinking skills such as the ability to design, evaluate, generalize, and analyse information rather than simply recall it.
6 Introduce Topics in manifold representations.
7 Show the different ways to solve the same problem with different circuits/logic and encourage the students to come up with their own creative ways to solve them.
8 Discuss how every concept can be applied to the real world - and when that's possible, it helps improve the students' understanding.

Module-1

Introduction: Causes of Energy Scarcity, Solution to Energy Scarcity, Factors Affecting Energy Resource Development, Energy Resources and Classification, Renewable Energy – Worldwide Renewable Energy Availability, Renewable Energy in India.

Energy from Sun: Sun- earth Geometric Relationship, Layer of the Sun, Earth – Sun Angles andtheir Relationships, Solar Energy Reaching the Earth's Surface, Solar Thermal Energy Applications.

Module-2

Solar Thermal Energy Collectors: Types of Solar Collectors, Configurations of Certain Practical Solar Thermal Collectors, Material Aspects of Solar Collectors, Concentrating Collectors, Parabolic Dish – Stirling Engine System, Working of Stirling or Brayton Heat Engine, Solar Collector Systems into Building Services, Solar Water Heating Systems, Passive Solar Water Heating Systems, Applications of Solar Water Heating Systems, Active Solar Space Cooling, Solar Air Heating, Solar Dryers, Crop Drying, Space Cooing, Solar Cookers, Solar pond.

Solar Cells: Components of Solar Cell System, Elements of Silicon Solar Cell, Solar Cell materials, Practical Solar Cells, I – V Characteristics of Solar Cells, Efficiency of Solar Cells, Photovoltaic panels (series and parallel arrays).

Module-3
Hydrogen Energy: Benefits of Hydrogen Energy, Hydrogen Production Technologies, Hydrogen Energy Storage, Use of Hydrogen Energy, Advantages and Disadvantages of Hydrogen Energy, Problems Associated with Hydrogen Energy. **Wind Energy:** Windmills, Wind Turbines, Wind Resources, Wind Turbine Site Selection. **Geothermal Energy:** Geothermal Systems, Classifications, Geothermal Resource Utilization, Resource Exploration, Geothermal Based Electric Power Generation, Associated Problems, environmental Effects. **Solid waste and Agricultural Refuse:** Waste is Wealth, Key Issues, Waste Recovery Management Scheme, Advantages and Disadvantages of Waste Recycling, Sources and Types of Waste, Recycling of Plastics.
Module-4
Biomass Energy: Biomass Production, Energy Plantation, Biomass Gasification, Theory of Gasification, Gasifier and Their Classifications, Chemistry of Reaction Process in Gasification, Updraft, Downdraft and Cross-draft Gasifiers, Fluidized Bed Gasification, Use of Biomass Gasifier, Gasifier Biomass Feed Characteristics, Applications of Biomass Gasifier, Cooling and Cleaning of Gasifiers. **Biogas Energy:** Introduction, Biogas and its Composition, Anaerobic Digestion, Biogas Production, Benefitsof Biogas, Factors Affecting the Selection of a Particular Model of a Biogas Plant, Biogas Plant Feeds and theirCharacteristics. **Tidal Energy:** Introduction, Tidal Energy Resource, Tidal Energy Availability, Tidal Power Generation in India, Leading Country in Tidal Power Plant Installation, Energy Availability in Tides, Tidal Power Basin, Turbines for Tidal Power, Advantages and Disadvantages of Tidal Power, Problems Faced in Exploiting Tidal Energy.
Module-5
Sea Wave Energy: Introduction, Motion in the sea Waves, Power Associated with Sea Waves, Wave Energy Availability, Devices for Harnessing Wave Energy, Advantages and Disadvantages of Wave Power. **Ocean Thermal Energy:** Introduction, Principles of Ocean Thermal Energy Conversion (OTEC), Ocean Thermal Energy Conversion plants, Basic Rankine Cycle and its Working, Closed Cycle, Open Cycle and Hybrid Cycle, Carnot Cycle, Application of OTEC in Addition to Produce Electricity, Advantages, Disadvantages and Benefits of OTEC.
Course outcome (Course Skill Set) At the end of the course the student will be able to : 1. Discuss causes of energy scarcity and its solution, energy resources and availability of renewable energy. Outline energy from sun, energy reaching the Earth's surface and solar thermal energy applications. 2. Discuss types of solar collectors, their configurations, solar cell system, its characteristics and their applications. 3. Explain generation of energy from hydrogen, wind, geothermal system, solid waste and agriculture refuse. 4. Discuss production of energy from biomass, biogas. 5. Summarize tidal energy resources, sea wave energy and ocean thermal energy.
Assessment Details (both CIE and SEE) The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). The student is declared as a pass in the course if he/she secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

- There are 25 marks for the CIE's Assignment component and 25 for the Internal Assessment Test component.
- Each test shall be conducted for 25 marks. The first test will be administered after 40-50% of the coverage of the syllabus, and the second test will be administered after 85-90% of the coverage of the syllabus. The average of the two tests shall be scaled down to 25 marks
- Any two assignment methods mentioned in the 22OB2.4, if an assignment is project-based then only one assignment for the course shall be planned. The schedule for assignments shall be planned properly by the course teacher. The teacher should not conduct two assignments at the end of the semester if two assignments are planned. Each assignment shall be conducted for 25 marks. (If two assignments are conducted then the sum of the two assignments shall be scaled down to 25 marks)
- The final CIE marks of the course out of 50 will be the sum of the scale-down marks of tests and assignment/s marks.

Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester-End Examination:

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (**duration 03 hours).**

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
3. The students have to answer 5 full questions, selecting one full question from each module.
4. Marks scored shall be proportionally reduced to 50 marks.

Suggested Learning Resources:

Books

Textbook

1. Nonconventional Energy Resources, Shobh Nath Singh, Pearson, 1st Edition, 2015.

Reference Books

1. Nonconventional Energy Resources, B.H. Khan, McGraw Hill, 3rd Edition.
2. Renewable Energy; Power for a sustainable Future, Godfrey Boyle, Oxford, 3rd Edition, 2012.
3. Renewable Energy Sources: Their Impact on global Warming and Pollution, Tasneem Abbasi S.A. Abbasi, PHI,1st Edition, 2011.

Web links and Video Lectures (e-Resources):

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Activity Based Learning (Suggested Activities in Class)/ Practical Based learning

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Industrial Servo Control Systems		Semester	VI
Course Code	**BEE654C**	CIE Marks	50
Teaching Hours/Week (L:T:P: S)	3:0:0:0	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	03	Exam Hours	03
Examination type (SEE)	Theory		

Course objectives:

(1) To explain the evolution and classification of servos, with descriptions of servo drive actuators, amplifiers, feedback transducers, performance, and troubleshooting techniques.
(2) To discuss system analogs and vectors, with a review of differential equations.
(3) To discuss the concept of transfer functions for the representation of differential equations.
(4) To discuss mathematical equations for electric servo motors, both DC and brushless DC servo motors.
(5) To represent servo drive components by their transfer function, to combine the servo drive building blocks intosystem block diagrams.
(6) To determine the frequency response techniques for proper servo compensation.

Teaching-Learning Process (General Instructions)

These are sample Strategies, which teachers can use to accelerate the attainment of the various course outcomes.

1 Lecturer method (L) needs not to be only traditional lecture method, but alternative effective teaching methods could be adopted to attain the outcomes.
2 Use of Video/Animation to explain functioning of various concepts.
3 Encourage collaborative (Group Learning) Learning in the class.
4 Ask at least three HOT (Higher order Thinking) questions in the class, which promotes critical thinking.
5 Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop design thinking skills such as the ability to design, evaluate, generalize, and analyse information rather than simply recall it.
6 Introduce Topics in manifold representations.
7 Show the different ways to solve the same problem with different circuits/logic and encourage the students to come up with their own creative ways to solve them.
8 Discuss how every concept can be applied to the real world - and when that's possible, it helps improve the students' understanding.

Module-1

Servos: Introduction, Benefits of Servo Systems, Types of Servos - Evolution of Servo Drives, Classification of Drives, Components of Servos - Hydraulic/Electric Circuit Equations, Actuators- Electric, Actuators-Hydraulic,Amplifiers-Electric,Amplifiers-Hydraulic,Transducers (Feedback).

Module-2

Machine Servo Drives: Types of Drives, Feed Drive Performance.
Troubleshooting Techniques: Techniques by Drive, Problems: Their Causes and Cures.
Machine Feed Drives: Advances in Technology, Parameters for making Application Choices.
Application of Industrial Servo Drives: Introduction, Physical System Analogs, Quantities and Vectors, Differential Equations for Physical Systems, Electric Servo Motor Transfer Functions and Time Constants, Transport Lag Transfer Function, Hydraulic Servo Motor Characteristics, General Transfer Characteristics

Module-3

Generalized Control Theory: Servo Block Diagrams, Frequency-Response Characteristics and Construction of Approximate (Bode) Frequency Charts, Nichols Charts, Servo Analysis Techniques, Servo Compensation.
Indexes of Performance: Definition of Indexes of Performance for Servo Drives, Indexes of Performance for Electric and Hydraulic Drives.

Module-4

Performance Criteria: Percent Regulation, Servo System Responses.
Servo Plant Compensation Techniques: Dead-Zone Nonlinearity, Change-in-Gain Nonlinearity, Structural Resonances, Frequency Selective Feedback, Feed forward Control. Machine Considerations: Machine feed drive Considerations, Ball Screw Mechanical Resonances and Reflected Inertias for Machine Drives.

Module-5
Machine Considerations: Drive Stiffness, Drive Resolution, Drive Acceleration, Drive Speed Considerations, Drive Ratio Considerations, Drive Thrust/Torque And Friction Considerations, Drive Duty Cycles.
Course outcome (Course Skill Set) 1. Explain the evolution and classification of servos, with descriptions of servo drive actuators, amplifiers,feedback transducers, performance, and troubleshooting techniques. 2. Discuss system analogs, vectors and transfer functions of differential equations. 3. Discuss mathematical equations for electric servo motors, both DC and brushless DC servo motors. 4. Represent servo drive components by their transfer function, to combine the servo drive building blocksinto system block diagrams.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). The student is declared as a pass in the course if he/she secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

- There are 25 marks for the CIE's Assignment component and 25 for the Internal Assessment Test component.
- Each test shall be conducted for 25 marks. The first test will be administered after 40-50% of the coverage of the syllabus, and the second test will be administered after 85-90% of the coverage of the syllabus. The average of the two tests shall be scaled down to 25 marks
- Any two assignment methods mentioned in the 22OB2.4, if an assignment is project-based then only one assignment for the course shall be planned. The schedule for assignments shall be planned properly by the course teacher. The teacher should not conduct two assignments at the end of the semester if two assignments are planned. Each assignment shall be conducted for 25 marks. (If two assignments are conducted then the sum of the two assignments shall be scaled down to 25 marks)
- The final CIE marks of the course out of 50 will be the sum of the scale-down marks of tests and assignment/s marks.

Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester-End Examination:

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (**duration 03 hours).**

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
3. The students have to answer 5 full questions, selecting one full question from each module.
4. Marks scored shall be proportionally reduced to 50 marks.

Suggested Learning Resources:

Books

Textbook

1. Industrial Servo Control Systems Fundamentals and Applications, George W. Younkin, Marcel Dekker, 1stEdition, 2003.

Reference Books

1. Servo Motors and Industrial Control Theory, Riazollah Firoozian, Springer, 2nd Edition, 2014.
2. DC SERVOS Application and Design with MATLAB, Stephen M. Tobin, CRC, 1st Edition, 2011.

Web links and Video Lectures (e-Resources):

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Activity Based Learning (Suggested Activities in Class)/ Practical Based learning

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SEMICONDUCTOR DEVICES		Semester	VI
Course Code	BEE654D	CIE Marks	50
Teaching Hours/Week (L:T:P: S)	3:0:0:0	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	03	Exam Hours	03
Examination nature (SEE)	Theory		

Course objectives:

Courseobjectives:

1)To learn basics of various types of power electronic devices
2)To study Snubber circuits for the protection of power semiconductor devices.
3)To learn gate and base drive circuits for power semiconductor devices
4) To develop a heat sink to control the temperature rise of semiconductor devices
5)Learn to design magnetic components inductors and transformers used in the power electronic circuits

Teaching-Learning Process (General Instructions)

These are sample Strategies, which teachers can use to accelerate the attainment of the various course outcomes.

. These are sample Strategies, which teacher can use to accelerate the attainment of the various course
outcomes and make Teaching –Learning more effective

1. Lecturer method (L) does not mean only the traditional lecture method, but a different type of teaching method may be adopted to develop the outcomes.
2. Show Video/animation films to explain the functioning of various analog and digital circuits.
3. Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop thinking skills such as the ability to evaluate, generalize, and analyse information rather than simply recall it.
4. Show the different ways to solve the same problem and encourage the students to come up with their own creative ways to solve them.
5. Discuss how every concept can be applied to the real world - and when that's possible, it helps improve the students' understanding

Module-1

Power Electronics: Introduction, Converter Classification, Power Electronics Concepts, Electronic Switches, Switch Selection, Spice, PSpice and Capture, Representation of switches in Pspice -The Voltage-Controlled Switch, Transistors, Diodes and Thyristors (SCRs).

Power Computations: Introduction, Power and Energy, Inductors and Capacitors, Energy Recovery, Effective Values, Apparent Power and Power Factor, Power Computations for Sinusoidal AC Circuits, Power Computations for Nonsinusoidal Periodic Waveforms, Power Computations Using Pspice.

Basic Semiconductor Physics: Introduction, Conduction Processes in Semiconductors pn Junctions, Charge Control Description of pn-Junction Operation, Avalanche Breakdown

Module-2

Power Diodes: Introduction, Basic Structure and I – V characteristics, Breakdown Voltage Considerations, On –State Losses, Switching Characteristics, Schottky Diodes.
Bipolar Junction Transistors: Introduction, Vertical Power Transistor Structures, Z-V Characteristics, Physics of BJT Operation, Switching Characteristics, Breakdown Voltages, Second Breakdown, On-State Losses, Safe Operating areas.
Power MOSFETs : Introduction, Basic Structure, I-V Characteristics, Physics of Device Operation, Switching Characteristics, Operating Limitations and Safe Operating Areas

Module-3

Thyristors: Introduction, Basic Structure, I-V Characteristics, Physics of Device Operation, Switching Characteristics, Methods of Improving di/dt and dv/dt Ratings.
Gate Turn-Off Thyristors: Introduction, Basic Structure and Z-V Characteristics,
Physics of Turn-Off Operation, GTO Switching Characteristics, Overcurrent Protection of GTOs.
Insulated Gate Bipolar Transistors: Introduction, Basic Structure, I-V Characteristics, Physics of Device Operation, Latchup in IGBTs, Switching Characteristics, Device Limits and SOAs.
Emerging Devices and Circuits: Introduction, Power Junction Field Effect Transistors, Field-Controlled Thyristor, JFET-Based Devices versus Other Power Devices, MOS-Controlled Thyristors, Power Integrated Circuits, New Semiconductor Materials for Power Devices

Module-4

Snubber Circuits: Function and Types of Snubber Circuits, Diode Snubbers, Snubber Circuits for Thyristors, Need for Snubbers with Transistors, Turn-Off Snubber, Overvoltage Snubber, Turn-On Snubber, Snubbers for Bridge Circuit Configurations, GTO Snubber Considerations.
Gate and Base Drive Circuits: Preliminary Design Considerations, dc-Coupled Drive Circuits, Electrically Isolated Drive Circuits, Cascode-Connected Drive Circuits, Thyristor Drive Circuits, Power Device Protection in Drive Circuits, Circuit Layout Considerations

Module-5

Component Temperature Control and Heat Sinks: Control of Semiconductor Device Temperatures, Heat Transfer by Conduction, Heat sinks, Heat Transfer by Radiation and Convection.
Design of Magnetic Components: Magnetic Materials and Cores, Copper Windings, Thermal Considerations, Analysis of a Specific Inductor Design, Inductor Design Procedures, Analysis of a Specific Transformer Design, Eddy Currents, Transformer Leakage Inductance, Transformer Design Procedure, Comparison of Transformer and Inductor Sizes

Course outcome (Course Skill Set)

At the end of the course the student will be able to:
1) Discuss power electronic concepts, electronic switches and semiconductor physics.
2) Explain representation of switches in P-spice and power computations.
3) Explain the internal structure, the principle of operation, characteristics and base drive circuits of power semiconductor devices; power diodes, power BJT, power MOSFET.
4) Explain the internal structure, the principle of operation, characteristics and base drive circuits of power semiconductor devices; thyristors, power IGBT, power FET

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

- For the Assignment component of the CIE, there are 25 marks and for the Internal Assessment Test component, there are 25 marks.
- The first test will be administered after 40-50% of the syllabus has been covered, and the second test will be administered after 85-90% of the syllabus has been covered
- Any two assignment methods mentioned in the 22OB2.4, if an assignment is project-based then only one assignment for the course shall be planned. The teacher should not conduct two assignments at the end of the semester if two assignments are planned.
- For the course, CIE marks will be based on a scaled-down sum of two tests and other methods of assessment.

Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester-End Examination:

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (**duration 03 hours).**

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
3. The students have to answer 5 full questions, selecting one full question from each module.
4. Marks scored shall be proportionally reduced to 50 marks

Suggested Learning Resources:

Books

1. Power Electronics, Daniel W Hart, McGraw Hill.
2. Power Electronics Converters, Applications, and Design, Ned Mohan et al, Wiley, 3rd Edition, 2014.
3. Semiconductor Device Modeling with Spice, G. Massobrio, P. Antognetti, McGraw-Hill, 2nd Edition, 2010.
4. Power Semiconductor Devices, B. JayantBaliga, Springer, 2008.
5. Power Electronics Principles and Applications, Joseph Vithayathil, McGraw-Hill, 2011.

Web links and Video Lectures (e-Resources):

. Youtube videos NPTEL lecturers
Activity Based Learning (Suggested Activities in Class)/ Practical Based learning Seminars Quiz Assignments

B. E. ELECTRICAL AND ELECTRONICS ENGINEERING
Choice Based Credit System (CBCS) and Outcome Based Education (OBE)
SEMESTER – VI

CONTROL SYSTEM LABORATORY

Course Code	**BEEL606**	CIE Marks	50
Number of Practical Hours/Week(L:T:P)	0:2:2	SEE Marks	50
Credits	01	Exam Hours	03

Course Learning Objectives:

- To draw the speed torque characteristics of AC and DC servo motor.
- To determine the time and frequency reposes of a given second order system using discrete components.
- To design and analyze Lead, Lag and Lag – Lead compensators for given specifications.
- To study the feedback control system and to study the effect of P, PI, PD andPID controller and Lead compensator on the step response of the system.
- To simulate and write a script files to plot root locus, bode plot, to study the stability of the system

Sl. NO	Experiments
1	Experiment to draw the speed torque characteristics of (i) AC servo motor (ii) DC servo motor
2	Experiment to draw synchro pair characteristics
3	Experiment to determine frequency response of a second order system
4	(a) To design a passive RC lead compensating network for the given specifications, viz, the maximum phase lead and the frequency at which it occurs and to obtain the frequency response.
5	(a) To design a passive RC lag compensating network for the given specifications, viz, the maximum phase lag and the frequency at which it occurs and to obtain the frequencyresponse. (b) To determine experimentally the transfer function of the lag compensating network
6	Experiment to draw the frequency response characteristics of the lag – lead compensator network and determination of its transfer function.
7	To study a second order system and verify the effect of (a) P, (b) PI, (c) PD and (d) PID controller on the step response.
8	(a) To simulate a typical second order system and determine step response and evaluate time response specifications. (b) To evaluate the effect of adding poles and zeros on time response of second order system. (c) To evaluate the effect of pole location on stability
9	(a) To simulate a D.C. Position control system and obtain its step response. (b) To verify the effect of input waveform, loop gain and system type on steady state errors. (c) To perform trade-off study for lead compensator. (d) To design PI controller and study its effect on steady state error.
10	(a) To examine the relationship between open-loop frequency response and stability, open-loop frequency and closed loop transient response (b) To study the effect of open loop gain on transient response of closed loop system using root locus.
11	(a) To study the effect of open loop poles and zeros on root locus contour (b) Comparative study of Bode, Nyquist and root locus with respect to stability.

Note:

Sl.	Description	Experiment numbers
1	Perform experiments using suitable components/equipment's	1 & 2
2	Perform experiments using suitable components/equipment's and verify the results using standard simulation package	3,4,5,6 and 7
3	Perform simulation only using standard package	8,9,10 and 11

Course Outcomes: At the end of the course the student will be able to:

- Utilize software package and discrete components in assessing the time and frequency domain response of a given second order system.
- Design, analyze and simulate Lead, Lag and Lag – Lead compensators for given specifications.
- Determine the performance characteristics of ac and DC servomotors and synchro-transmitter receiver pair used in control systems.
- Simulate the DC position and feedback control system to study the effect of P, PI, PD and PID controller and Lead compensator on the step response of the system.
- Develop a script files to plot Root locus, Bode plot and Nyquist plot to study the stability of

Conduct of Practical Examination:

1. All laboratory experiments are to be included for practical examination.
2. Breakup of marks and the instructions printed on the cover page of answer script to be strictly adhered by the examiners.
3. Students can pick one experiment from the questions lot prepared by the examiners.
4. Change of experiment is allowed only once and 15% Marks allotted to the procedure part to be made zero.

Energy Management in Electric Vehicles		Semester	VI
Course Code	BEE657A	CIE Marks	50
Teaching Hours/Week (L:T:P: S)	1:0:0:0	SEE Marks	50
Total Hours of Pedagogy	15	Total Marks	100
Credits	01	Exam Hours	01
Examination type (SEE)	MCQ		

Course objectives:

- To provide a comprehensive understanding of energy management principles and strategies specific to electric vehicles.
- To familiarize students with the various components and systems involved in energy management in electric vehicles.
- To equip students with the knowledge and skills to apply optimization techniques for efficient energy management in electric vehicles.

Teaching-Learning Process (General Instructions)

These are sample Strategies, which teachers can use to accelerate the attainment of the various course outcomes.

1. Interactive Lectures: Conduct interactive lectures where the instructor presents the theoretical concepts, principles, and case studies related to energy management in electric vehicles.
2. Case Studies and Projects: Assign case studies and projects that require students to apply the concepts and strategies learned in class to real-world scenarios.
3. Guest Lectures and Industry Visits: Invite guest speakers from the industry or research organizations who are experts in the field of energy management in electric vehicles.

Module-1

Introduction to Electric Vehicles and Energy Management Overview of electric vehicles (EVs) - Types of EVs (Battery Electric Vehicles, Plug-in Hybrid Electric Vehicles); Advantages and challenges of EVs. Introduction to energy management in EVs - Importance of energy management; Key objectives of energy management in EVs. Electric vehicle components and systems- Battery systems; Power electronics and motor drive systems; Regenerative braking systems; Energy storage and management systems

Module-2

Fundamentals of Energy Management Energy storage technologies for EVs - Lithium-ion batteries; Solid-state batteries; Supercapacitors; Fuel cells. Battery charging and discharging techniques - Charging infrastructure for EVs; Charging modes (AC and DC charging); Fast charging vs. slow charging; Battery management systems (BMS). Energy efficiency and energy loss analysis - Losses in power electronics and motor drive systems; Losses in battery systems; Factors affecting energy efficiency in EVs.

Module-3

Advanced Energy Management Strategies State-of-charge (SoC) estimation and management - SoC estimation techniques (Coulomb counting, Kalman filtering, etc.); SoC balancing techniques; Impact of SoC on battery life and performance. Power management strategies - Optimal power allocation between different vehicle systems; Dynamic power allocation based on driving conditions; Power flow control in EVs. Regenerative braking and energy recovery - Principles of regenerative braking; Control strategies for regenerative braking; Energy recovery and utilization.

Module-4
Optimization Techniques for Energy Management Optimization models for energy management - Linear programming and nonlinear optimization; Model predictive control (MPC) for energy management; Genetic algorithms and other heuristic optimization techniques. Intelligent energy management systems - Artificial intelligence (AI) and machine learning techniques for energy management; Reinforcement learning-based energy management; Data-driven approaches for energy optimization. Realtime energy management algorithms - Real-time optimization algorithms for energy allocation; Adaptive control strategies for energy management; Integration of energy management with navigation systems.
Module-5
Case Studies and Applications Energy management in electric buses and fleet management - Challenges and strategies for energy management in public transportation; Fleet management and scheduling optimization. Energy management in electric vehicles charging infrastructure - Smart charging stations and grid integration; Demand-side management and load balancing. Emerging trends and future directions in energy management - Wireless charging technologies; Vehicle-to-vehicle (V2V) communication for energy optimization; Advanced energy storage and conversion technologies.
Course outcome (Course Skill Set) At the end of the course the student will be able to: 1. Understand and analyse the energy storage technologies used in electric vehicles. 2. Understand the design and implementation of energy management strategies for electric vehicles, considering factors such as battery charging, power allocation and regenerative braking. 3. Understand optimization techniques and intelligent algorithms to optimize energy management in electric vehicles, considering real-time constraints and factors such as driving conditions and energy efficiency goals.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). The student is declared as a pass in the course if he/she secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together

Continuous internal Examination (CIE)

- For the Assignment component of the CIE, there are 25 marks and for the Internal Assessment Test component, there are 25 marks.
- The first test will be administered after 40-50% of the syllabus has been covered, and the second test will be administered after 85-90% of the syllabus has been covered
- Any two assignment methods mentioned in the 22OB2.4, if an assignment is project-based then only one assignment for the course shall be planned. The teacher should not conduct two assignments at the end of the semester if two assignments are planned.
- For the course, CIE marks will be based on a scaled-down sum of two tests and other methods of assessment.

Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester End Examinations (SEE)

SEE paper shall be set for 50 questions, each of the 01 marks. The pattern of the question paper is MCQ (multiple choice questions). The time allotted for SEE is **01 hour.** The student has to secure a minimum of 35% of the maximum marks meant for SEE.

Suggested Learning Resources:

Books

1. "Electric Vehicle Technology" by H. C. Rai
2. "Electric Vehicle Energy Management System for Efficiency Optimization" by Jingang Han, Linlin Tan, and Xinbo Ruan
3. "Advanced Electric Drive Vehicles" edited by Ali Emadi
4. "Electric Vehicle Technology Explained" by James Larminie and John Lowry

Web links and Video Lectures (e-Resources):

- makes.mindmatrix.io

Activity Based Learning (Suggested Activities in Class)/ Practical Based learning

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Simulation and Control of Power Electronics Circuits		Semester	
Course Code	BEEL657B	CIE Marks	50
Teaching Hours/Week (L:T:P: S)	0-0-1	SEE Marks	50
Credits	01	Exam Hours	100
Examination type (SEE)	practical/Viva-Voce		

Course objectives:

- To be able to simulate any DC-DC converter and observe the performance under various test conditions
- To be able to simulate single phase and three phase DC –AC converters and observe the performance under various test conditions
- To be able to simulate uncontrolled, half controlled and fully controlled AC-DC converters and observe the performance under various test conditions

Sl.NO	Experiments
1	(a)Simulate a single phase half wave diode bridge rectifier. Input 100V, 50 Hz. AC supply. At the out put, resistance of 50 ohms. (b)Simulate a single phase full wave diode bridge rectifier. Input 100V, 50 Hz. AC supply. At the out put, resistance of 50 ohms.
2	(a) Simulate a single phase half controlled full wave rectifier. Input 100V, 50 Hz. AC supply. At the out put, resistance of 50 ohms. (b) Simulate a single phase fully controlled full wave rectifier. Input 100V, 50 Hz. AC supply. At the out put, resistance of 50 ohms.
3	Simulate a buck converter with 20 V DC input, and regulate the output at 10 V by implementing a PI controller for closed loop operation. The out put power to vary from 10 W to 20 W. Ensure that voltage ripple is limited to 1%.
4	Simulate a boost converter with 20 V DC input, and regulate the output at 35 V by implementing a PI controller for closed loop operation. The out put power to vary from 30W to 60 W. Ensure that voltage ripple is limited to 1%
5	Simulate a single phase AC voltage controller using a triac with 100V ,50 Hz. AC supply for an RL load of 10 oms and 2 mH.
6	Simulate a three phase inverter with 180 degree conduction mode with DC input of 100V and a star connected balanced resistive of 40 ohms each. Use IGBT for inverter.
7	Simulate a single phase SPWM inverter with 50V DC input with modulation indices of 0.5, 0.6 and 0.8. connect a resistance of 25 ohms at the output of inverter. Use power Mosfets for inverter.
8	Simulate a three phase inverter with 120 degree mode of conduction. Take input DC voltage of 100V and three phase star connected balanced resistive load of 50 ohms each.
	Demonstration Experiments (For CIE)
9	In expt. 8. connect suitable LC filter at the output to obtain a sinusoidal output with THD of less than 8 %.

10	Simulate a three phase SPWM inverter with 50V DC input with modulation indices of 0.5, 0.6 and 0.8. connect a star connected resistances of 25 ohms each at the output of the inverter. Use power Mosfets for inverter.
11	Simulate a three phase, 5 level, neutral point clamped (NPC) inverter. Input DC voltage is 100V. The inverter output is connected to a balanced 3 phase resistive load of 40 Ohms each.
12	Simulate a forward converter with input DC voltage of 30 V. Take transformer ratio of 1.5:1. Observe the output voltages for duty cycles of 0.4, 0.6 and 0.8. Ensure that the output voltage ripple is less than 0.5 V. The load resistance is 10 Ohms.

Course outcomes (Course Skill Set):

At the end of the course the student will be able to:

- Simulate any given power electronic circuit and evaluate its performance under different test conditions and also observe the performance for different values of passive filtering elements used in the converter.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation (CIE):

CIE marks for the practical course are **50 Marks**.

The split-up of CIE marks for record/ journal and test are in the ratio **60:40**.

- Each experiment is to be evaluated for conduction with an observation sheet and record write-up. Rubrics for the evaluation of the journal/write-up for hardware/software experiments are designed by the faculty who is handling the laboratory session and are made known to students at the beginning of the practical session.
- Record should contain all the specified experiments in the syllabus and each experiment write-up will be evaluated for 10 marks.
- Total marks scored by the students are scaled down to **30 marks** (60% of maximum marks).
- Weightage to be given for neatness and submission of record/write-up on time.
- Department shall conduct a test of 100 marks after the completion of all the experiments listed in the syllabus.
- In a test, test write-up, conduction of experiment, acceptable result, and procedural knowledge will carry a weightage of 60% and the rest 40% for viva-voce.
- The suitable rubrics can be designed to evaluate each student's performance and learning ability.
- The marks scored shall be scaled down to **20 marks** (40% of the maximum marks).

The Sum of scaled-down marks scored in the report write-up/journal and marks of a test is the total CIE marks scored by the student.

Semester End Evaluation (SEE):

- SEE marks for the practical course are 50 Marks.
- **SEE shall be conducted by the two examiners. One from the same institute as an internal examiner and another from a different institute as an external examiner, appointed by the university.**
- The examination schedule and names of examiners are informed to the university before the conduction of the examination. These practical examinations are to be conducted between the schedule mentioned in the

academic calendar of the University.

- All laboratory experiments are to be included for practical examination.
- (Rubrics) Breakup of marks and the instructions printed on the cover page of the answer script to be strictly adhered to by the examiners. **OR** based on the course requirement evaluation rubrics shall be decided jointly by examiners.
- Students can pick one question (experiment) from the questions lot prepared by the examiners jointly.
- Evaluation of test write-up/ conduction procedure and result/viva will be conducted jointly by examiners.

General rubrics suggested for SEE are mentioned here, writeup-20%, Conduction procedure and result in -60%, Viva-voce 20% of maximum marks. SEE for practical shall be evaluated for 100 marks and scored marks shall be scaled down to 50 marks (however, based on course type, rubrics shall be decided by the examiners)

Change of experiment is allowed only once and 15% of Marks allotted to the procedure part are to be made zero.

The minimum duration of SEE is 02 hours

Suggested Learning Resources:

https://in.mathworks.com/solutions/electrification/power-electronics-simulation.html

- - This provides design examples for power electronics simulation using MATLAB

Energy Audit Project		Semester	
Course Code	**BxxLxxx**	CIE Marks	50
Teaching Hours/Week (L:T:P: S)		SEE Marks	50
Credits	01	Exam Hours	03
Examination type (SEE)	Practical		

Course objectives:

- Along with prescribed hours of teaching –learning process, provide opportunity to perform the experiments/programmes at their own time, at their own pace, at any place as per their convenience and repeat any number of times to understand the concept.
- Provide unhindered access to perform whenever the students wish.
- Vary different parameters to study the behaviour of the circuit without the risk of damaging equipment / device or injuring themselves.
- To carryout Energy Audit for an industry, business establishment, organization and its computation using
- Scilab Software and proposing possible remedial measures to reduce the energy consumption.

Students shall select real time project/audit with the approval of the guide. The following shall be considered by the students and guide while auditing.

(1) Building and Utility Data Analysis: The main purpose of this step is to evaluate the characteristics of the energy systems and the patterns of energy use for the premises considered. The premises characteristics can be collected from the architectural/ mechanical/electrical drawings and/or from consultation/discussions with premises operators. The energy use patterns can be obtained from a compilation of utility bills over a period.

(2) Walk-Through Survey: This step should identify potential energy savings measures. The results of this stepare important since they determine if the building warrants any further energy auditing work. Some of the tasks involved in this step are • Identify the customer's concerns and needs • Check the current operating and maintenance procedures • Determine the existing operating conditions of major energy use equipment (lighting,HVAC systems, motors, etc.) • Estimate the occupancy, equipment, and lighting (energy use density and hours of operation).

(3)Baseline for Building Energy Use: The main purpose of this step is to develop a base-case model that represents the existing energy use and operating conditions for the building. This model will be used as a reference to estimate the energy savings due to appropriately selected energy conservation measures.

Evaluation of Energy-Saving Measures: In this step, a list of cost-effective energy conservation measures is determined using both energy savings and economic analysis.

Based on the ability/abilities of the student/s and recommendations of the mentor, a single discipline or a multidisciplinary project under ability enhancement can be assigned to an individual student or to a group havingnot more than 4 students.

Assessment Details (both CIE and SEE)

CIE procedure for project ability enhancement course:

(i) Single discipline: The CIE marks shall be awarded by a committee consisting of the Head of the concernedDepartment and two senior faculty members of the Department, one of whom shall be the Guide. The CIE marks awarded for the project work, shall be based on the evaluation of project report, project presentation skill and question and answer session in the ratio 50:25:25.The marks awarded for the project reportshall be the same for all the batch mates.

Interdisciplinary: Continuous Internal Evaluation shall be group wise at the college level with the participation of all the guides of the college.

The CIE marks awarded for the project, shall be based on the evaluation of project report, project presentation skill and question and answer session in the ratio 50:25:25.The marks awarded for the project report shall be thesame for all the batch mates.

SEE for project:

(i) Single discipline: Contribution to the Mini-project and the performance of each group member shall be assessed individually in the semester end examination (SEE) conducted at the department.

(ii) Interdisciplinary: Contribution to the Mini-project and the performance of each group member shall be assessed individually in semester end examination (SEE) conducted separately at the departments to which the student/s belong to.

The SEE marks awarded for the project, shall be based on the evaluation of project report, project presentation skill and question and answer session in the ratio 50:25:25.The marks awarded for the project report shall be thesame for all the batch mates.

Course outcomes (Course Skill Set):

At the end of the course the student will be able to:

- Analyze the data collected for energy audit of a building or industry or organization.
- Perform comparative analysis with and without energy audit.
- Analyze the energy saving measures to be considered with economy considerations.
- Analyse in a systematic way, think better, and perform better

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation (CIE):

CIE marks for the practical course are **50 Marks**.

The split-up of CIE marks for record/ journal and test are in the ratio **60:40**.

- Each experiment is to be evaluated for conduction with an observation sheet and record write-up. Rubrics for the evaluation of the journal/write-up for hardware/software experiments are designed by the faculty who is handling the laboratory session and are made known to students at the beginning of the practical session.
- Record should contain all the specified experiments in the syllabus and each experiment write-up will be evaluated for 10 marks.
- Total marks scored by the students are scaled down to **30 marks** (60% of maximum marks).
- Weightage to be given for neatness and submission of record/write-up on time.
- Department shall conduct a test of 100 marks after the completion of all the experiments listed in the syllabus.
- In a test, test write-up, conduction of experiment, acceptable result, and procedural knowledge will carry a weightage of 60% and the rest 40% for viva-voce.
- The suitable rubrics can be designed to evaluate each student's performance and learning ability.
- The marks scored shall be scaled down to **20 marks** (40% of the maximum marks).

The Sum of scaled-down marks scored in the report write-up/journal and marks of a test is the total CIE marks scored by the student.

Semester End Evaluation (SEE):

- SEE marks for the practical course are 50 Marks.
- **SEE shall be conducted by the two examiners. One from the same institute as an internal examiner and another from a different institute as an external examiner, appointed by the university.**
- The examination schedule and names of examiners are informed to the university before the conduction of the examination. These practical examinations are to be conducted between the schedule mentioned in the academic calendar of the University.
- All laboratory experiments are to be included for practical examination.
- (Rubrics) Breakup of marks and the instructions printed on the cover page of the answer script to be strictly adhered to by the examiners. **OR** based on the course requirement evaluation rubrics shall be

decided jointly by examiners.

- Students can pick one question (experiment) from the questions lot prepared by the examiners jointly.
- Evaluation of test write-up/ conduction procedure and result/viva will be conducted jointly by examiners.

General rubrics suggested for SEE are mentioned here, writeup-20%, Conduction procedure and result in -60%, Viva-voce 20% of maximum marks. SEE for practical shall be evaluated for 100 marks and scored marks shall be scaled down to 50 marks (however, based on course type, rubrics shall be decided by the examiners)

Change of experiment is allowed only once and 15% of Marks allotted to the procedure part are to be made zero.

The minimum duration of SEE is 02 hours

Suggested Learning Resources:

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Project on Renewable Energy Sources		Semester	VI
Course Code	BEEL657D	CIE Marks	50
Teaching Hours/Week (L:T:P: S)	0:0:2:0	SEE Marks	50
Credits	01	Exam Hours	03
Examination type (SEE)	Practical		

Course objectives:

- Along with prescribed hours of teaching –learning process, provide opportunity to perform the experiments/programmes at their own time, at their own pace, at any place as per their convenience and repeat any number of times to understand the concept.
- Provide unhindered access to perform whenever the students wish.
- Vary different parameters to study the behavior of the circuit without the risk of damaging equipment/ deviceor injuring themselves.

Students can select appropriate projects with the approval of the guide. The projects be applicationoriented and can be considering any of the following or any other.

Automatic solar tracking system.
Solar based small traffic control system.
Solar mobile charger.
Vertical axis wind turbine system.
Solar powered Smart irrigation system.
Renewable energy based home automation system.
Domestic illumination using solar.
Solar grass cutter.
Solar UPS.

Course outcomes (Course Skill Set):

At the end of the course the student will be able to:

(1) Analyse in a systematic way, think better, and perform better.

Based on the ability/abilities of the student/s and recommendations of the mentor, a single discipline or a multidisciplinary project under ability enhancement can be assigned to an individual student or to a group having not more than 4 students.

Assessment Details (both CIE and SEE)

CIE procedure for project ability enhancement course:

(i) Single discipline: The CIE marks shall be awarded by a committee consisting of the Head of the concerned Department and two senior faculty members of the Department, one of whom shall be the Guide.

The CIE marks awarded for the project work, shall be based on the evaluation of project report, project presentation skill and question and answer session in the ratio 50:25:25.The marks awarded for the project report shall be the same for all the batch mates.

(ii) Interdisciplinary: Continuous Internal Evaluation shall be group wise at the college level with the participation of all the guides of the college.

The CIE marks awarded for the project, shall be based on the evaluation of project report, project presentation skill and question and answer session in the ratio 50:25:25.The marks awarded for the project report shall be the same for all the batch mates.

SEE for project:

(i) Single discipline: Contribution to the Mini-project and the performance of each group member shall be assessed individually in the semester end examination (SEE) conducted at the department.

(ii) Interdisciplinary: Contribution to the Mini-project and the performance of each group member shall be assessed individually in semester end examination (SEE) conducted separately at the departments to which the student/s belong to.

The SEE marks awarded for the project, shall be based on the evaluation of project report, project presentation skill and question and answer session in the ratio 50:25:25.The marks awarded for the project report shall be the same for all the batch mates.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation (CIE):

CIE marks for the practical course are **50 Marks**.

The split-up of CIE marks for record/ journal and test are in the ratio **60:40**.

- Each experiment is to be evaluated for conduction with an observation sheet and record write-up. Rubrics for the evaluation of the journal/write-up for hardware/software experiments are designed by the faculty who is handling the laboratory session and are made known to students at the beginning of the practical session.
- Record should contain all the specified experiments in the syllabus and each experiment write-up will be evaluated for 10 marks.
- Total marks scored by the students are scaled down to **30 marks** (60% of maximum marks).
- Weightage to be given for neatness and submission of record/write-up on time.
- Department shall conduct a test of 100 marks after the completion of all the experiments listed in the syllabus.
- In a test, test write-up, conduction of experiment, acceptable result, and procedural knowledge will carry a weightage of 60% and the rest 40% for viva-voce.
- The suitable rubrics can be designed to evaluate each student's performance and learning ability.
- The marks scored shall be scaled down to **20 marks** (40% of the maximum marks).

The Sum of scaled-down marks scored in the report write-up/journal and marks of a test is the total CIE marks scored by the student.

Semester End Evaluation (SEE):

- SEE marks for the practical course are 50 Marks.
- **SEE shall be conducted by the two examiners. One from the same institute as an internal examiner and another from a different institute as an external examiner, appointed by the university.**
- The examination schedule and names of examiners are informed to the university before the conduction of the examination. These practical examinations are to be conducted between the schedule mentioned in the academic calendar of the University.
- All laboratory experiments are to be included for practical examination.
- (Rubrics) Breakup of marks and the instructions printed on the cover page of the answer script to be strictly adhered to by the examiners. **OR** based on the course requirement evaluation rubrics shall be decided jointly by examiners.
- Students can pick one question (experiment) from the questions lot prepared by the examiners jointly.
- Evaluation of test write-up/ conduction procedure and result/viva will be conducted jointly by examiners.

General rubrics suggested for SEE are mentioned here, writeup-20%, Conduction procedure and result in -60%, Viva-voce 20% of maximum marks. SEE for practical shall be evaluated for 100 marks and scored marks shall be scaled down to 50 marks (however, based on course type, rubrics shall be decided by the examiners)

Change of experiment is allowed only once and 15% of Marks allotted to the procedure part are to be made zero.

The minimum duration of SEE is 02 hours

Suggested Learning Resources:

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